

# Rigorous Stability Criterion for Digital Phase Locked Loops

Brian Daniels and Ronan Farrell

*Abstract*—This paper proposes a rigorous stability criterion for an arbitrary order digital phase locked loop (DPLL), with a charge pump phase frequency detector (CP-PFD) component. Stability boundaries for such systems are determined using piecewise linear methods to model the non-linear nature of the CP-PFD component block. The model calculates the control voltage, after a predetermined number of input reference signal sampling periods, to a small initial voltage offset. This paper, in particular, takes an in-depth look at the second order system. The second order stability boundaries, as defined by the proposed technique, are compared to that of existing linear theory stability boundaries, and display a significant improvement. The applicability of the proposed technique to higher order systems, using a numerically iterative solution, is presented. Finally the proposed methodology is used to determine the stability boundary of a third order system and thus the component values for a stable system. Using these component values the response of the DPLL to an initial control voltage offset is simulated using a circuit level simulation.

*Index Terms*—High Order, Phase Locked Loop, Piecewise Linear, Stability.

## I. INTRODUCTION

The Digital Phase Locked Loop (DPLL) is a versatile component block widely used in electronics for operations such as frequency synthesis and clock data recovery. The DPLL system considered in this paper consists of a bang bang phase frequency detector (PFD), a charge pump (CP), a voltage controlled oscillator (VCO), and a low pass loop filter (LF), with a structure as shown in fig. 1.

Manuscript received March 25, 2008. Research presented in this paper was funded by a Centre for Telecommunications Value-Chain Research (SFI 03/CE3/I405) by Science Foundation Ireland under the National Development Plan, and by the Enterprise Ireland Commercialisation Fund. The authors gratefully acknowledge this support.

B. Daniels is with the Institute of Microelectronics and Wireless Systems, National University of Ireland Maynooth, Maynooth, County Kildare, Ireland, (e-mail: bdaniels@eeng.nuim.ie)

R. Farrell is with the Centre for Telecommunications Value-Chain Research, National University of Ireland Maynooth, Maynooth, County Kildare, Ireland, (e-mail: rfarrell@eeng.nuim.ie)

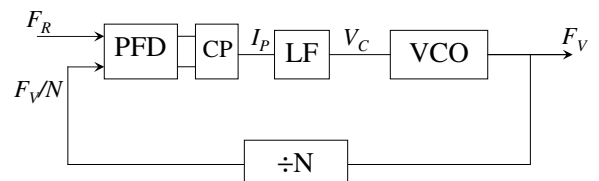


Fig. 1. DPLL Loop Block Diagram

The DPLL loop uses a local oscillator reference signal to generate a robust signal at the output of the VCO. The phase of the reference and feedback signals are compared by the PFD and any difference is represented as a current on the charge pump output,  $I_P$ . This error drives the VCO output signal towards that of the reference, and thus drives the loop towards lock.

The most basic type of PLL, a first order PLL, has no loop filter and thus it is globally stable. But it produces large frequency jitter or phase noise on the output signal that is intolerable for most applications. It is normal practice to include a loop filter to reduce this jitter. Ideally the higher the order of filter the lower the phase noise on the output signal. However the inclusion of a loop filter introduces stability concerns that now need to be considered during the design process [1]. Because of these stability issues it is considered risky to design DPLL systems of order greater than third. Thus the second and third order DPLLs are the most common PLLs designed today. The DPLL loop filter structure for the third order loop is shown in fig. 2. In the case of a second order DPLL the capacitor  $C_3$  is removed. This paper aims to provide an alternative methodology that enables the design of high order systems by accurately determining their stability boundaries. To achieve this, a number of issues need to be considered; first the nonlinearity of the DPLL loop; and second the complexity of the higher order DPLL linear equations.

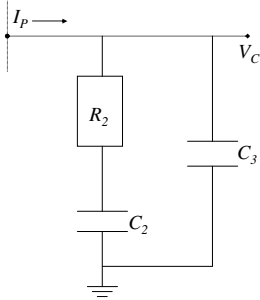


Fig. 2. Third Order DPLL filter Structure

The nonlinearities of the DPLL system exist in the CP-PFD and the VCO component blocks. The VCO can be assumed linear if the DPLL system operates away from the saturation regions of the VCO. The non-linearity in the PFD is due to quantization-like effects at the output of the PFD. This non-linearity is inherent to the operation of the loop and cannot be ignored if an accurate model is required. Due to this inherent non-linearity, linearization, which ignores this quantization, is not entirely accurate. Thus it is generally the case that empirical design and simulation are used concurrently to ensure the correct behaviour. This design methodology is outlined graphically in the flow chart of fig. 3. Traditionally the designer starts with a linear model and then applies rule of thumb or empirical simulation design techniques to redefine the system parameters.

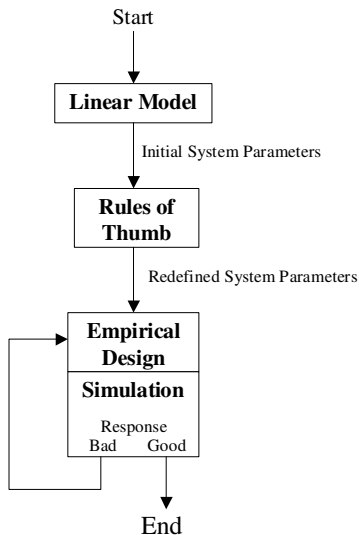


Fig. 3. Traditional Design Method

The alternative to the above, are nonlinear stability methods, however these are found to be unwieldy and further complicate the design of an already complex system. For this reason non-linear methods have only rarely been applied to the design of PLL systems [2-5]. There are other means of stabilising the DPLL by using advanced architecture techniques, for example gear-shifting [6,7], or aided acquisition dual-loops [8,9]. Gear-shifting varies the

loop bandwidth, from a fast locking wide bandwidth loop when the PLL is out of lock, to a low noise narrow bandwidth loop when loop lock is detected. Similarly dual-loops achieve fast lock and low noise using two feedback loops simultaneously, one loop has a wide bandwidth to allow fast lock and the second loop has narrow bandwidth for a low noise signal output.

This paper proposes a novel arbitrary-order stability criterion using piecewise linear methods to accurately model the inherent non-linear nature of the CP-PFD. The stability criterion is applicable to all orders of the DPLL system described earlier, with model equations given for each order of system from second through to fifth. In the case of the second order system a closed form solution of the stability criterion is determined, whereas numerical iteration is used to solve the equations for higher orders. The stability boundary is found for the second and third order DPLLs, and compared to the results from existing published linear models. In the next section traditional DPLL design techniques are considered. In section III the proposed piecewise linear model is introduced. Section IV takes, as an example, a more detailed look at the second order system and determines the stability boundary for this system. This boundary is compared to that of the linear model defined boundary of Gardner [1]. In section V the piecewise linear model's applicability to high orders is considered. Finally in section VI conclusions are presented.

## II. TRADITIONAL DESIGN TECHNIQUES

Traditionally the DPLL is linearised by replacing the PFD component with a subtractor component block in the analysis. This can be justified if the time-varying nature of the PFD is overlooked. This is a reasonable approximation when considering the PLL to be close to lock. In this situation it's key state variable, the VCO control voltage, changes by only a small amount on each cycle of the reference signal. This is known as the continuous time approximation and is valid when the loop bandwidth is small relative to the reference frequency, or more specifically no greater than  $1/10^{\text{th}}$  of the reference frequency [1]. This assumes that the detailed behaviour of the loop within each cycle is not important and only the average behaviour over many cycles is important. By applying an averaged analysis, the time-varying operation can be bypassed and linear analysis can be applied. The DPLL system of fig. 1 is approximated by the linear system block diagram as shown in fig. 4.

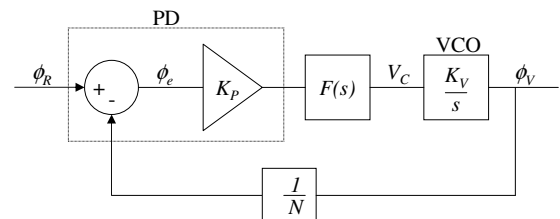


Fig. 4. Linear PLL (LPLL) system

The feedback frequency divider is used in frequency synthesis to produce an output signal frequency that is some multiple of the reference signal,  $N$  times  $F_R$  in fig. 1. The inclusion of a feedback divider scales  $F_V$  by  $N$ . In our analysis the divider introduces a scaling factor, however in this paper the feedback divide ratio is chosen to be equal to 1 for clarity. The transfer function of the LPLL system of fig. 4 is then given by:

$$H_{CL}(s) = \frac{K_V I_P F(s)}{2\pi s + K_V I_P F(s)} \quad (1)$$

where  $I_P$  is the charge pump current gain,  $K_V$  is the VCO gain and  $F(s)$  is the loop filter transfer function. Using (1), Gardner [1] identifies the stability boundary for the second order PLL system to be:

$$K' = \frac{1}{\frac{\pi}{\omega_R \tau_2} \left( 1 + \frac{\pi}{\omega_R \tau_2} \right)} \quad (2)$$

A plot of the stability boundary from equation (2) for a defined filter time constant  $\tau_2$ , and a range of reference frequencies ( $\omega_R$  radians/second) are shown in fig. 5.

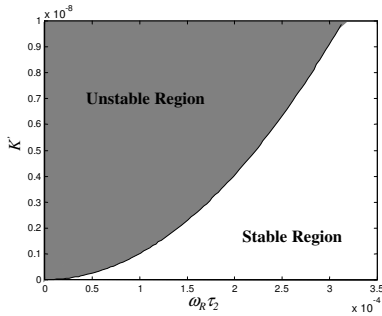


Fig. 5. Second order Gardner Stability Boundary

For the 3<sup>rd</sup> order system Gardner offers a similar stability boundary as defined by (3).

$$K' < \frac{4(1+a)}{b\omega_R \tau_2 \left[ \frac{2\pi(1+a)}{\omega_R \tau_2} + \frac{2(1-a)(b-1)}{b} \right]} \quad (3)$$

where,  $b = 1 + \frac{C_2}{C_3}$  and  $a = e^{-\frac{2\pi b}{\omega_R \tau_2}}$ .

Unlike Gardner [1] other linear stability criteria such as [10-12], do not provide a global prediction of the DPLL stability boundary. Instead they offer specific system parameter values from a chosen loop performance, such as the settling time [10], the phase margin [11], or the undamped natural frequency and damping factor [12]. These linear methods ignore the nonlinearities inherent in the CP-PFD, however they do provide a starting point from which empirical design methods are used to choose optimum component values and to insure that the DPLL will operate

as expected. In the next section an alternative stability criterion is proposed. This technique does not linearise the CP-PFD and thus determines a more accurate prediction of the DPLL stability boundary, allowing for more aggressive design.

### III. PIECEWISE LINEAR MODEL

In this section a novel piecewise linear model is proposed. This model is used later to determine the stability boundaries of the high order DPLL. As discussed earlier there are two issues that need to be considered; the CP-PFD nonlinearity and the complexity of the high order loop equations. The proposed methodology considers the nonlinearity of the CP-PFD, by using a state transition diagram to model the changing states of the CP-PFD. The high order model complexity is reduced by approximating the charge on the loop filter capacitors, removing differential terms, and thus simplifying the system equations, making it mathematically feasible to increment the model to high orders. For illustrative purposes this section pays particular attention to the second order system, the equivalent expressions for higher order systems are given in appendix A.

The proposed model assumes a small initial VCO control voltage offset  $V_o$  and determines the system stability from the state space response to this offset.  $V_o$  is chosen to be small for two reasons. First the error introduced by the model is directly proportional to  $V_o$ , and second a small  $V_o$  ensures that the maximum phase offset remains within the  $\pm \pi$  region, avoiding cycle slip events. Cycle slips occur when the feedback signal falling edge, to which the reference signal falling edge is being compared, changes, this incurs a  $2\pi$  shift in the phase error. These phenomena occur when the system is substantially out of lock and in acquisition mode. Cycle slip events can be explained by this analysis but are beyond the scope of this paper.

In fig. 6 a plot of the state space system trajectory is shown, where the two state variables are the phase error  $\phi_e$  and the control voltage  $V_C$ . For a stable system with a reference frequency equal to the VCO free running frequency  $F_{FR}$ , and an initial control voltage offset of  $V_o$ , the system will settle to the equilibrium of the origin, shown as the dashed line in fig. 6.

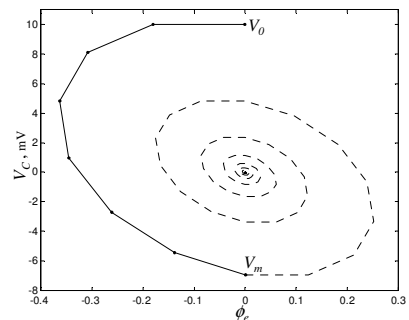


Fig. 6. State Space Plot of Stable System

The continuous curve in fig. 6 is a piecewise linear curve where the dots correspond to samples of the VCO control voltage. In the case of the second order DPLL, the system is linear between these sample points, allowing the piecewise linear method to give an exact calculation of this state space curve. This is not the case with higher order systems as differential equations need to be solved to determine the response between these sample points. Such higher order systems are solved here using numerical iteration of the charge approximated equations given in appendix A. The continuous line of fig. 6 is one half cycle of the state space curve. If the value of  $V_m$ , which is the first zero crossing of  $\phi_e(t)$ , can be calculated, then the system stability can be determined as follows: if  $|V_m| > V_0$  then the system trajectory is diverging and is therefore unstable; If  $|V_m| < V_0$  then the trajectory is converging and is stable. The calculation of  $\phi_e(t)$  and  $V_C(t)$  depends on the filter's charge approximated difference equations. For the second order system  $\phi_e(t)$  and  $V_C(t)$  are determined using the set of difference equations (4) and (5). For higher order PLLs additional state variables need to be considered, specifically the charge on each additional filter capacitor. However if  $V_C(t)$  reaches a stable equilibrium then the filter capacitor state variables have also reached the equilibrium. Therefore when considering the stability of a high order system, we need only monitor  $\phi_e(t)$  and  $V_C(t)$ .

$$V_C(t_{n+1}) = V_C(t_n) - \frac{I_P T_B}{C_2} \quad (4)$$

$$\phi_e(t_{n+1}) = \phi_e(t_n) + 2\pi \left( T(F_R - F_{FR}) - (K_V \int V_C dt) \right) \quad (5)$$

where  $F_{FR}$  is the VCO free running frequency, and  $K_V$  is the VCO gain,  $T$  is the reference signal time period, and  $T_B$  is defined here as the boost time of the CP-PFD or the length of time during each period  $T$  where the CP-PFD pumps a non zero current into the loop filter. To further clarify consider one time period,  $T$ , of the loop. In this time period the DPLL operates in the coast state, where no current is output from the CP-PFD, for a period of time defined here as  $T_C$ , and in boost state for a period of  $T_B$ , as in fig. 7.  $T_B$  is calculated as in equation (6).

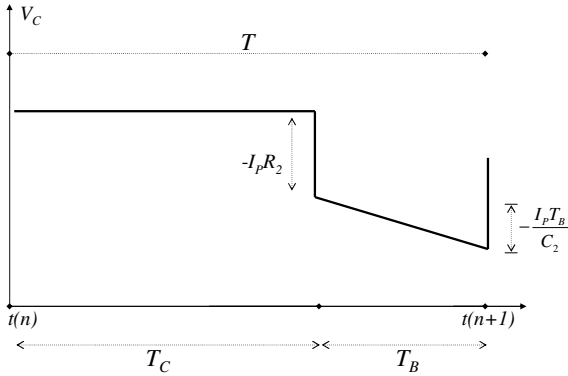


Fig. 7. One Period of  $V_C$  for 2<sup>nd</sup> Order DPLL

$$T_B = \left| \frac{\phi_e(t_n) T}{2\pi} \right| \quad (6)$$

where  $\phi_e(t_n)$  is the phase error at time  $t_n$ . The coast time period is calculated as  $T_C = T_B - T$ . Once the time periods are calculated,  $V_C$  can be determined using (4). To solve equation (5) an estimate of the integral of  $V_C$  is required. For the second order DPLL, the loop filter is first order, and therefore the integration corresponds to a linear ramp and can be expressed as:

$$\int V_C dt = TV_C(t_n) - T_B I_P R_2 - \frac{T_B^2 I_P}{2C_2} \quad (7)$$

As discussed earlier high order DPLLs have high order differential terms in their system equations, thus finding a closed form solution equivalent to the second order equations above becomes a difficult task. The solution suggested here is to approximate the high order system equations using charge approximation as presented in [13]. This approach converts a set of parallel integral equations into a set of linear difference equations. It considers the charge on each capacitor rather than the voltage at each node, making the assumption that the average current  $I_{avg}$  through a capacitor during the period  $\Delta t$ , which is unknown, is equal to the current at time  $t$ ,  $I(t)$ , as in fig. 8.

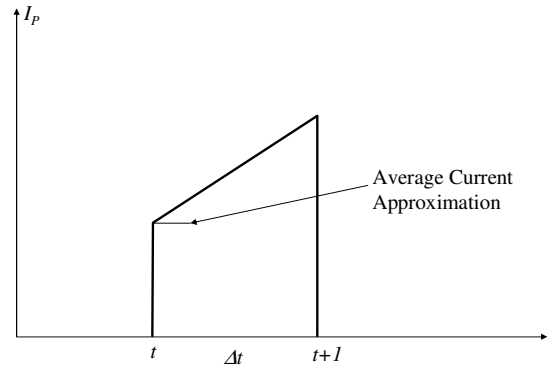


Fig. 8. Assumption that current at time  $t$  is equal to the average current during  $\Delta t$

Utilising charge approximation, the complexity is reduced making it possible to derive closed form solutions to higher order DPLL systems. This can be justified for high frequency systems as a large  $F_R$  will result in a small period  $T$ , making the approximation more accurate. For clarity consider the third order system before charge approximation is applied as in equation (8).

$$V_C(t+1) = I_P R_2 - C_3 R_2 \frac{dV_C}{dt} + \frac{1}{C_2} \int I_P dt - \frac{C_3}{C_2} V_C(t) \quad (8)$$

This equation is complicated by differential and integral terms, as the order increases the equivalent  $V_C$  solution becomes increasingly complex. Using charge approximation this equation can be rewritten as those given in equations (A1), (A3) and (A4) from appendix A. While these

equations may appear to be more expansive they do not have any differential terms. The benefit is more significant for 5<sup>th</sup> and 6<sup>th</sup> order systems as they cannot be solved in closed form without making such an approximation. The error introduced due to this approximation is bounded and tends to zero as the time interval  $\Delta t$  tends to zero, as shown in fig. 9(a) and fig. 9(b). For large reference frequencies or a small initial  $V_C$  offset  $\Delta t$ , the error due to the charge approximation is minimal. The relevant charge approximated difference equations for a number of filters of increasing order are given in appendix A.

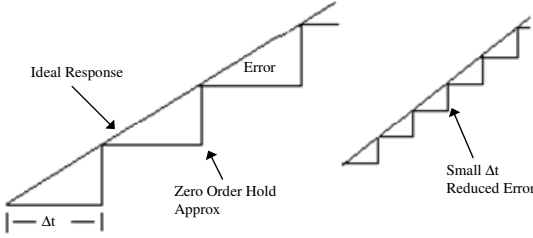


Fig. 9. (a) Zero order hold approximation with large  $\Delta t$ , (b) smaller  $\Delta t$  smaller Error

This model is a significant improvement over existing methods in that it is more accurate and results in simpler system equations, due to a combination of the piecewise linear method and the charge approximation. Using the methodology described in this section it is possible to determine the stability boundaries for any DPLL system by numerically iterating the charge approximated system equations given in appendix A, for a small initial VC offset, by looking at the system trajectory over a short period of time as shown in fig. 6. This is achievable for any order of DPLL system using numerical iteration; however it is possible to determine a closed form stability criterion for the second order system by extending the methodology described here. This is considered in the next section.

#### IV. SECOND ORDER PIECEWISE LINEAR MODEL

In this section a more detailed consideration of the piecewise linear model, in the case of the second order DPLL, is given. This approach determines the second order DPLL control voltage after  $m$  periods of the reference signal,  $V_m$ , as defined in fig. 6. The solution of  $V_m$  is used to define a closed form solution of the DPLL stability boundary for the second order system.

To determine  $V_m$  two things need to be considered: first, when all parameters are known, any  $n^{\text{th}}$  sample of the control voltage  $V_n$  needs to be calculated in closed form; and second the number of samples  $m$  needs to be calculated where  $V_m$  is the control voltage at the first zero crossing of the phase error as shown in fig. 6. These two requirements are considered in the following two subsections.

##### 1) Calculation of $V_n$

The second order system, described by equations (4), and (5) can be reduced to the pair of summations given in (9) and (10), where  $V_0$  is an initial positive  $V_C$  offset, the initial  $\phi_e$  offset is zero, and  $\phi_e$  is always negative as in fig. 6.

$$V_C(n) = V_0 + \frac{I_p T}{2\pi C_2} \sum_{j=0}^{n-1} \phi_e(j) \quad (9)$$

$$\phi_e(j) = -2\pi K_V T \sum_{k=0}^{j-1} (1 - K_V T I_P R_2)^{j-k-1} V_C(k) \quad (10)$$

Equations (9) and (10) may be combined to give:

$$V_n = V_0 - \frac{K_V I_p T^2}{C_2} \sum_{j=0}^{n-1} \sum_{k=0}^{j-1} (1 - K_V I_P R_2 T)^{j-k-1} V_C(k) \quad (11)$$

where  $V_n$  is equivalent to  $V_C(n)$  and is an exact calculation of the control voltage after  $n$  samples. The double summation in equation (11) can be solved by either numerical iteration, or by solving a closed form simplification. This closed form solution is considered later in subsection 3.

The control voltage at the zero crossing,  $V_m$  will not correspond exactly with  $V_n$ , as the last sample  $n$  will not fall exactly on the phase error zero crossing, but will cross that line by some value  $d$ , as shown in fig. 10. If samples  $n-1$  and  $n$  are both known then it is possible to calculate the value of  $V_m$  by using a linear interpolation (12).

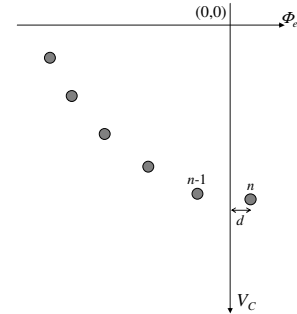


Fig. 10. State Space Samples

$$V_m = V_y - \phi_y \frac{|V_x| - |V_y|}{|\phi_x| + |\phi_y|} \quad (12)$$

where  $(V_x, \phi_x)$  and  $(V_y, \phi_y)$  are the co-ordinates of the samples  $n$  and  $n-1$  respectively in fig. 10. However (12) is not used in this model as the error introduced in the calculation of  $V_m$  is minimal and reduces as the reference frequency is increased.

##### 2) Calculation of number of samples $m$

To calculate the number of samples  $m$  it is necessary to return to the linear approximation model and use the linear error transfer function:

$$H_e(s) = \frac{C_2 s^2}{C_2 s^2 + K_V I_P R_2 C_2 s + K_V I_P} \quad (13)$$

Using linear theory to determine  $m$  does not reduce the accuracy of this technique, as we only require an approximate value of  $m$  and then round it up to the next

integer. To determine the phase error zero crossings the frequency step response of (13) is calculated and the inverse Laplace taken as shown in (14) and equated to zero.

$$L^{-1}\left(\frac{2\pi\Delta_F}{s^2}H_e(s)\right)=0 \quad (14)$$

where  $\Delta_F$  is the frequency step size. Solving (14) gives an equation of the form  $A(t)\sin(X(t))=0$ , which is zero when  $X(t)=0, \pi, 2\pi, 3\pi, \dots$ . The first zero crossing after  $t=0$  occurs when  $X(t)=\pi$ . Solving this gives equation (15), the time of the first zero crossing.

$$t_m = \frac{2\pi}{\sqrt{(K_V I_P (4 - K_V I_P R_2^2 C_2)) / C_2}} \quad (15)$$

The number of samples in one half cycle of the state space trajectory, (the solid arc of the system trajectory in fig. 6) is estimated as:

$$m = \lceil t_m F_R + 1 \rceil = \left\lceil \frac{2\pi F_R}{\sqrt{(K_V I_P (4 - K_V I_P R_2^2 C_2)) / C_2}} + 1 \right\rceil \quad (16)$$

### 3) Closed Form Solution of $V_m$

The value of  $V_m$ , the control voltage at the first zero crossing of the phase error, can be found using equations (11) and (16) and numerical iteration. However it is also possible to solve equation (11) in closed form, as shown below.

$$V_m = V_0 \begin{bmatrix} 1 + A(\Lambda_1) \\ + A^2(\Lambda_2) \\ + A^3(\Lambda_3) \\ \vdots \\ + A^{\lceil \frac{m}{2} \rceil}(\Lambda_{\lceil \frac{m}{2} \rceil}) \end{bmatrix} \quad (17)$$

where  $A = -K_V I_P / (F_R^2 C_2)$  and  $\Lambda_1$  up to  $\Lambda_{\lceil m/2 \rceil}$  are a set of parameters defined as equations (B1-B5) from appendix B. Since parameter  $|A|$  is always  $\ll 1$ , a further simplification can be made. As  $F_R^2$  is a large number,  $|A|$  becomes less significant as the power of  $A$  is increased. In fact it is found that terms with powers of  $A$  greater than 4 are insignificant and have negligible influence on the final value of  $V_m$ . So (17) can be simplified to:

$$V_m = V_0 [1 + A(\Lambda_1) + A^2(\Lambda_2) + A^3(\Lambda_3) + A^4(\Lambda_4)] \quad (18)$$

Now that the phase error at the zero crossing can be determined, it is possible to determine the stability boundary of the second order DPLL using the calculation of the system parameter  $V_m$  in equation (18) and an estimate of  $m$  in (16).

An important system performance criterion is the pull-in rate. Using the system trajectory, as in fig. 6 and  $V_m$ , the system pull-in rate can be determined for an initial VCO control voltage offset  $V_0$ .

$$P_m = 100 \frac{V_0 + V_m}{V_0} \% \quad (19)$$

If the pull-in percentage is negative, the system is unstable otherwise the system is stable. Combining (18) and (19) the stability criterion can be simplified to:

$$2 + A\Lambda_1 + A^2\Lambda_2 + A^3\Lambda_3 + A^4\Lambda_4 > 0 \quad (20)$$

This is independent of the initial VCO control voltage offset  $V_0$ . As would be expected, the initial condition does not have any effect on the stability boundary. Equating (20) to zero gives the stability boundary of the system and can be compared to the traditional stability boundary of [1]. In fig. 11 the stability boundaries of the proposed second order technique are determined for a pull-in rate of 1%, 20% and 40% and are shown along with Gardner's linear boundary [1] and a stability boundary defined by a number of circuit level simulations. The accuracy of the circuit level simulation has been verified using other published behavioural and event driven DPLL models [14-16].

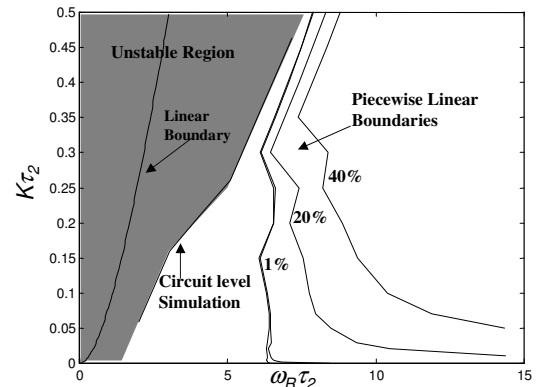


Fig. 11. Stability boundaries of 1GHz second order PLL according to Gardner and the proposed method

It is clear from fig. 11 that the circuit level model of the DPLL system suggests that Gardner's prediction is not conservative enough and does not guarantee stability. In fact there is a significant stable region defined by Gardner, where the circuit level model predicts instability. This discrepancy is the reason why DPLL designers need to complement linear design methods with rule of thumb and empirical design. The circuit level boundary also verifies that the proposed technique is more accurate, producing more conservative results than the linear boundary, which are inside the stability region of the DPLL system. Thus any DPLL system designed with parameters chosen from within this predicted boundary will be stable. This illustrates the inaccuracies of applying the linear model to the DPLL system, as described earlier. While comparing the proposed

technique to additional stability methods such as [10-12] is desirable, it is not possible due to the specific nature of these methods, and the difficulty in plotting any global stability boundary with such methods.

In this section the second order piecewise linear model, introduced in section III, was considered in more detail. The system initial conditions, the phase error and the control voltage, are chosen to be zero and some positive real value respectively.

### V. HIGHER ORDER SYSTEMS

The proposed piecewise linear technique can also be used to model higher orders by numerically iterating the relevant piecewise linear charge approximated equations as given in appendix A. The significant advantage of the charge approximation approach is that it removes differential terms from the filter equations and makes the solution of higher order DPLL system equations mathematically feasible.

Using the piecewise linear model the stability boundary is found for the 3<sup>rd</sup> order DPLL and compared to the traditional boundaries of [1]. In fig. 12, the stability boundaries for the 3<sup>rd</sup> order system are plotted for various values of  $b$ , where  $b = I + C_2/C_3$ . This definition of  $b$  is originally given in [1].

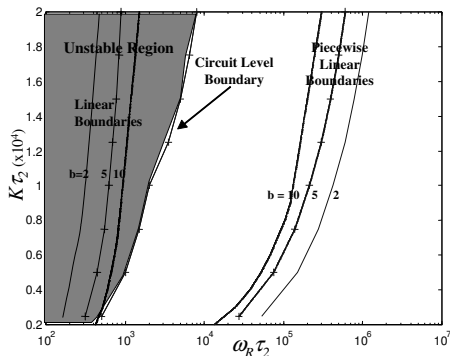


Fig. 12. 3<sup>rd</sup> Order Stability Boundaries for  $b = 2, 5, \text{ and } 10$

Similar to the second order case, fig. 12 illustrates the weakness of the linear boundaries. To further illustrate this consider an example using the proposed technique to define the stability boundary of a third order DPLL with a 1 GHz reference signal, a divide ratio of 1 and a value of  $b$  equal to 8. The predicted boundary is plotted in fig. 13, along with the stability boundary as defined by Gardner.

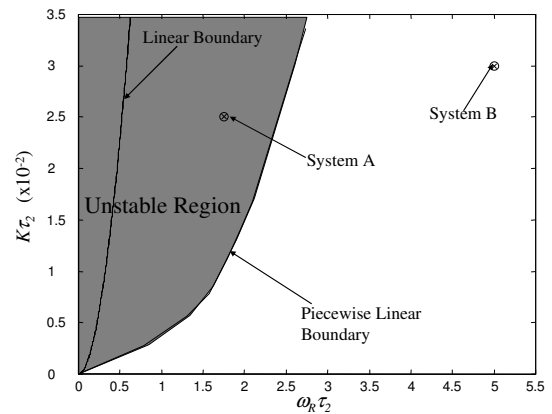


Fig. 13. Predicted Stability Boundary for 1 GHz system

The shaded section is the unstable region of the DPLL. Using this prediction of the boundary, two systems are considered, system A and B as defined in fig. 13. System A lies in the region between the predicted piecewise linear boundary and Gardner's, with a choice of  $K\tau_2$  and  $\omega_R\tau_2$  of 0.025 and 1.75 respectively. System B is well within the stable region with a choice of  $K\tau_2$  and  $\omega_R\tau_2$  of 0.03 and 5 respectively. The response of both systems are determined using the circuit level simulation described earlier. The response of systems A and B are shown in fig. 14 and fig. 15 below.

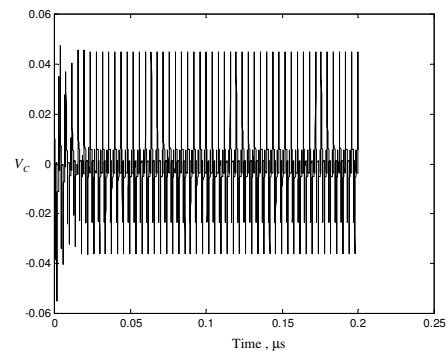


Fig. 14. Response of System A

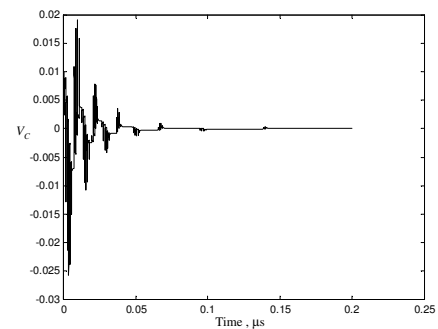


Fig. 15. Response of System B

We can see that as predicted the DPLL response of system A is unstable, yet this is counter to Gardner's prediction of stability. In the case of system B the system is found to be stable (fig. 15). It is clear from fig. 12 and the above example that, similar to the second order system, the third order piecewise linear technique provides a much better prediction of the stability boundary than linear methods. While it has yet to be proved conclusively, our initial results indicate that this is also true for other high order systems.

## VI. CONCLUSION

Traditional CP-PLL design techniques use linear theory and empirical methods to identify and design stable systems. It is shown in this paper that stability boundaries defined using traditional linear methods are inaccurate and use complicated model equations that are limited to low order loops. The proposed technique uses a charge approximation methodology applied to the loop filter equations. This removes the differential terms, simplifies the model, and enables the model to be incremented up to high orders. The proposed technique also uses piecewise linear methods to significantly increase the accuracy of the model relative to existing linear methods, and thus identify more accurate estimates of the stability boundary. This approach considers the exact nonlinear nature of the PFD, rather than simply approximating it to an adder component as in the linear case.

The paper concentrates, in particular, on the second order loop, defining a closed form solution of the stability boundary using linear integration. Though this solution is expansive, it is mathematically tractable and is found to better define the stable region of the DPLL. For systems with orders of greater than second, the loop filter equations can no longer be solved in closed form, but must be solved using a numerical iteration. The resulting model is a significant improvement over existing linear techniques, defining the system stability boundary more accurately for arbitrary order of the DPLL.

## APPENDIX

### Appendix A – High Order Piecewise Linear Equations

The third through fifth order piecewise linear model equations are outlined in the subsections below. In each of these cases, the control voltage  $V_C$  is determined from the charge on the filter capacitors, where  $Z$  is the system order.

$$V_C(t+1) = \frac{Q_Z(t+1)}{C_Z} \quad (A1)$$

The integral of  $V_C$ , to replace the second order calculation in (7), is calculated from the knowledge of  $V_C$  as shown in equation (A2).

$$\int V_C dt = T_B V_C(t) + \frac{I_Z(t+1)T_B^2}{2C_Z} \quad (A2)$$

### Third Order Difference Equations

$Q_2$  and  $Q_3$ , the charges on the loop filter capacitors,  $C_2$  and  $C_3$  respectively, are calculated as follows:

$$Q_2(t+1) = Q_2(t) - T_B(I_P - I_3(t+1)) \quad (A3)$$

$$Q_3(t+1) = Q_3(t) + T_B I_3(t+1) \quad (A4)$$

where  $T_B$  is equal to  $|\phi_e(k)/2\pi F_R|$  and  $I_3$  is calculated as:

$$I_3(t+1) = I_P - \frac{T_B^2 I_P C_2 + T_B C_2 C_3 \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right)}{T_B(C_2 + C_3) + R_2 C_2 C_3} \quad (A5)$$

### Fourth Order Difference Equations

For the fourth order system the charge on the loop filter capacitors are calculated as in equation (A6-A8).

$$Q_2(t+1) = Q_2(t)$$

$$+ \frac{T_B^2 I_3 C_2 - T_B C_2 C_3 \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right)}{T_B C_3 + R_2 C_2 C_3} \quad (A6)$$

$$Q_3(t+1) = Q_3(t) + T_B I_3 \quad (A7)$$

$$Q_4(t+1) = Q_4(t) + \frac{T_B^2 I_3 C_2 - T_B C_2 C_3 \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right)}{T_B C_3 + R_2 C_2 C_3} + T_B I_3 - T_B I_P \quad (A8)$$

where  $I_3$  and  $I_4$  are the current through  $C_3$  and  $C_4$  and are calculated as in equations (A9) and (A10).

$$I_3 = \frac{\left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right) - \left( \frac{Q_3(t)}{C_3} - \frac{Q_4(t)}{C_4} \right) + I_P}{\frac{R_2 + \frac{T_B}{C_2}}{C_2 T_B} + \frac{R_4 + \frac{T_B}{C_4}}{C_3 T_B + C_3 C_4 R_4} + 1} \quad (A9)$$

$$I_4 = I_P - I_3 - \frac{(I_3 C_2 T_B) - \left( C_2 C_3 \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right) \right)}{(C_3 T_B) + (C_2 C_3 R_2)} \quad (A10)$$

### Fifth Order Difference Equations

The fifth order loop filter capacitor charges are calculated as shown in equations (A11 - A14) given below.

$$Q_2(t+1) = Q_2(t) + I_2 T_B \quad (A11)$$

$$Q_3(t+1) = Q_3(t) + \frac{I_2 C_3 (R_2 C_2 + T) + C_3 Q_2(t) - C_2 Q_3(t)}{C_2 T} \quad (A12)$$

$$Q_4(t+1) = Q_4(t) - \frac{D_1}{D_2} + \frac{T(R_3 C_5 + T) \left( I_2 (R_2 C_2 + T) + C_2 T \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right) \right)}{C_2 T D_2} \quad (A13)$$

$$Q_5(t+1) = Q_5(t) + I_5 T_B \quad (A14)$$



where  $I_2$ ,  $I_5$  and  $D_1$  to  $D_4$  are defined as in equations (A15-A20) (Equation (A16) is at the bottom of this page).

$$I_2 = \frac{D_3 - D_4 \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right)}{1 + (R_2 C_2 + T) \frac{D_4}{C_2}} \quad (\text{A15})$$

$$D_2 = \frac{(R_3 C_3 + T)(R_4 C_4 + T) + C_4 R_3 T}{C_3} \quad (\text{A17})$$

$$D_1 = \left( \frac{Q_3(t)}{C_3} - \frac{Q_2(t)}{C_2} \right) (R_4 C_4 + T) + C_4 R_3 \left( \frac{Q_3(t)}{C_3} - \frac{Q_4(t)}{C_4} \right) \quad (\text{A18})$$

$$D_3 = \frac{D_1 (C_3 (R_4 C_4 + T) + C_4 T)}{D_2 C_3 (R_4 C_4 + T)} - I_p - \frac{C_4 \left( \frac{Q_3(t)}{C_3} - \frac{Q_2(t)}{C_2} \right)}{R_4 C_4 + T} \quad (\text{A19})$$

$$D_4 = \frac{C_2 C_3 T + T C_3 (R_4 C_4 + T) + C_4 T^2}{C_3 T D_2} \quad (\text{A20})$$

#### Appendix B – Closed Form Solution of $V_m$

This Section defines the parameters of  $\Lambda$  as used in equations (17) and (18).

$$\Lambda_1 = \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}^T \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & b & 0 & 0 & 0 \\ 1 & b & b^2 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ 1 & b & b^2 & \dots & b^{n-2} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \quad (\text{B1})$$

where  $b = 1 - (K_V R_2 I_P / F_R)$ .

$$\Lambda_2 = \begin{bmatrix} b^{n-4} + 2b^{n-5} + \dots + (n-4)b + (n-3) \\ b^{n-5} + 2b^{n-6} + \dots + (n-5)b + (n-4) \\ \vdots \\ b+2 \\ 1 \end{bmatrix}^T \quad (\text{B2})$$

$$\times \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & b & 0 & 0 & 0 \\ 1 & b & b^2 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ 1 & b & b^2 & \dots & b^{n-4} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}$$

If we consider  $\Lambda_3$  to be equal to the function  $\Gamma_k$  given in equation (B3) at the bottom of the page, where  $k = 6$ , then  $\Lambda_4$  can be calculated using equation (B4).

$$\Lambda_4 = \begin{bmatrix} \Gamma_8 \\ \Gamma_9 \\ \Gamma_{10} \\ \vdots \\ \Gamma_n \end{bmatrix}^T \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & b & 0 & 0 & 0 \\ 1 & b & b_2 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & b & b_2 & \dots & b_{n-8} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \quad (\text{B4})$$

It is possible to calculate all  $\Lambda$  up to  $\lceil m/2 \rceil$  by using the same process between equations (B2) and (B4), i.e. define  $\Gamma'_k$  as in equation (B5). Then  $\Lambda_5$  can be calculated as in (B6), and so on up to  $\Lambda_{\lceil m/2 \rceil}$ .

$$\Gamma'_k = \begin{bmatrix} \Gamma_k \\ \Gamma_{k+1} \\ \Gamma_{k+2} \\ \vdots \\ \Gamma_n \end{bmatrix}^T \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & b & 0 & 0 & 0 \\ 1 & b & b_2 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & b & b_2 & \dots & b_{n-k} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \quad (\text{B5})$$

$$I_5 = \frac{C_5 T^2 (R_5 C_5 + T) \left( I_2 (R_2 C_2 + T) + C_2 T \left( \frac{Q_2(t)}{C_2} - \frac{Q_3(t)}{C_3} \right) \right) - C_2 C_5 T^2 D_1 + C_2 C_5 T D_2 Q_4(t) - C_2 C_4 T D_2 Q_5(t)}{C_2 C_4 T D_2 (R_5 C_5 + T)} \quad (\text{A16})$$

$$\Gamma_k = \begin{bmatrix} b^{n-k} + 2b^{n-k-1} + \dots + (n-k)b + (n-k+1) \\ b^{n-k-1} + 2b^{n-k-2} + \dots + (n-k-1)b + (n-k) \\ \vdots \\ b+2 \\ 1 \end{bmatrix}^T \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & \frac{b+1}{b} & 0 & 0 & 0 \\ 1 & \frac{b+1}{b} & \frac{b^2+b+1}{b^2} & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ 1 & \frac{b+1}{b} & \frac{b^2+b+1}{b^2} & \dots & \frac{b^{n-k} + \dots + b+1}{b^{n-k}} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \quad (\text{B3})$$

$$\Lambda_5 = \begin{bmatrix} \Gamma'_{10} \\ \Gamma'_{11} \\ \Gamma'_{12} \\ \vdots \\ \Gamma'_n \end{bmatrix}^T \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & b & 0 & 0 & 0 \\ 1 & b & b_2 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & b & b_2 & \cdots & b_{n-10} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \quad (\text{B6})$$

## REFERENCES

- [1] Gardner, F.M., "Charge pump phase-lock loops," IEEE Trans. Commun., vol. COM-28, pp1849-1858, Nov 1980.
- [2] Abramovitch, D., "Lyapunov Redesign of Classical Digital Phase-Lock Loops", Proceedings of the American Control Conference Denver, Colorado, pp2401-2406, June 2003
- [3] Eva Wu, N., "Analog Phaselock Loop Design Using Popov Criterion", Proceedings of American Control Conf. Anchorage, pp16-18, May 2002
- [4] Rantzer, A., "Almost global stability of phase-locked loops", Proceedings of the 40th IEEE conf. On Decision and control, vol. 1, pp899-900, December 2001
- [5] Simon, D., El-Sherief, H., "Lyapunov Stability Analyses of Digital Phase Locked Loops", IEEE Conference on Systems, Man and Cybernetics, San Antonio, TX, pp2827-2829, October 1994.
- [6] Young-Shig Choi, Hyuk-Hwan Choi, Tae-Ha Kwon, "An Adaptive Bandwidth Phase Locked Loop with Locking Status Indicator", IEEE Russian-Korean International Symposium on Science and Technology, pp826-829, June 2005.
- [7] Yan Ge, Wennan Feng, Zhongjian Chen, Song Jia, Lijiu Ji, "A Fast Locking Charge-Pump PLL with Adaptive Bandwidth", IEEE Conf on ASIC, pp383-386, Oct. 2005.
- [8] Minoru Kamata, Takashi Shono, Takahiko Sabo, Iwao Sasase, and Shinsaku Mori, "Third-Order Phase-Locked Loops using Dual Loops with Improved Stability", IEEE J Solid-State Circuits, pp338-341, Aug. 1997
- [9] Carlosena, A., Manuel-Lazaro, A., "Design of High Order Phase-Lock Loops", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol 54, pp9-13, Jan. 2007
- [10] Mirabbasi, S., and Martin, K., "Design of Loop Filter in Phase-Locked Loops", IEEE Electronic Letters 1999, Vol. 35, Issue. 21, pp1801-1802
- [11] O'Keese, W., "An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump PLL's", National Semiconductor Application Note 1001, July 2001
- [12] Williamson, S., "How to Design RF Circuits – Synthesisers", IEE Colloquium on how to Design RF Circuits 2000.
- [13] Daniels, B., Farrell, R., Baldwin, G., "Arbitrary Order Charge Approximation Event Driven Phase Locked Loop Model", Irish Signals and Systems Conference, pp124 –128, June/July 2004
- [14] Van Paemel, M., "Analysis of a Charge-Pump PLL: A new Model", IEEE Trans on Communications, VOL.42, No 7, pp2490-2498, July 1994
- [15] Hedayat, C.D., Hachem, A., Leduc, Y., Benhassat, G., "High-level modeling applied to the second-order charge-pump PLL circuit", Texas Instruments Technical Journal, Vol 14, No. 2, March/April 1997
- [16] Hedayat, C.D., Hachem, A., Leduc, Y., Benhassat, G., "Modeling and Characterization of the 3rd Order Charge-Pump PLL: a Fully Event-driven Approach", Analog Integrated Circuits and Signal Processing, vol. 19, pp25-45, April 1999
- [17] Best, R., Phase Locked Loops Design, Simulation, and Applications, 4th edition, McGraw-Hill 1999
- [18] Abramovitch, D., "Phase-Locked Loops: A Control Centric Tutorial", Proceedings of the American Control Conference Anchorage, May 2002

**Brian Daniels** is currently a lecturer in Department of Electronic Engineering in NUI Maynooth. He has completed Masters in Telecommunications and a BEng degree, both from Dublin City University in 2001 and 1998 respectively. Before returning to do the Masters Brian worked in Ericsson for three years, specialising in designing and testing new software functions for the AXE10 mobile exchange on the PDC network.

Since 2001 he has been working in the Institute of Microelectronics and Wireless Electronics in the national university of Ireland Maynooth. As part of his graduate research Brian has been specialising in the modeling and design of digital phase locked loops.

**Ronan Farrell** is currently the Director of the Institute of Microelectronics and Wireless Systems in NUI Maynooth and an SFI theme leader for RF electronics and systems within the Centre for Telecommunications Value-Chain Driven Research (CTVR) which is the academic partner to Bell Labs Ireland. He graduated from University College Dublin in 1993 with a B.E. and proceeded to work with ICI/Zeneca Chemicals for the next two years in Louisiana, USA, and on various sites in Yorkshire, England. In 1995 he returned to University College Dublin to start a Masters on Sigma-Delta Modulators, sponsored by Analog Devices. This developed into a Ph.D. which he received in 1998. After receiving his Ph.D. he joined Parthus Technologies as a mixed signal IC designer. In 2001, he joined NUI Maynooth as a lecturer in the Department of Electronic Engineering. In 2004, he participated in the foundation of the SFI Centre for Telecommunications Value-Chain Driven Research (CTVR) which is the academic partner to Bell Labs Ireland. As of December 2005, Ronan was appointed director of the Institute of Microelectronics and Wireless Systems at NUI Maynooth. The Institute is a multidisciplinary centre focused on applied research in wireless systems and their enabling technologies. The institute has the objective of supporting both applied and fundamental research in the areas of wireless systems and microelectronics.