HARDWARE IMPLEMENTATION OF A VERSATILE LOW-COST MIXED-SIGNAL PLATFORM FOR SDR EXPERIMENTATION

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ABSTRACT

This paper presents the design of a reconfigurable mixed-signal platform used in the Software Defined Radio context. It is a single board part of a pre-existing modular system operating from 1.6 to 2.5 GHz that supports GSM1800, DCS1800, PCS1900, UMTS-FDD, UMTS-TDD and 802.11b standards. Its purpose is to facilitate configuration and data exchange between a computer and an RF transceiver. Technical choices, design and overall performances of the prototype are discussed.

1. INTRODUCTION

The concept of Software Defined Radio aims to provide reconfigurable radio systems able to cope with various existing or prospective telecommunication standards thanks to a single transceiver. This diversity is represented by the second generation (GSM, IS-95, DECT, PHS…) the 3G standards (such as W-CDMA, cdma2000, TD-CDMA) and the local area networks (like bluetooth, IEEE 802.11b). The commercial objective is to develop various applications implemented on standard hardware so as to avoid "stack radios". The main challenge for SDR is to optimise the tradeoffs between performance, power consumption and cost [1].

In order to make the architectural exploration of SDR systems easier, it is essential to provide flexible, versatile and reconfigurable systems to designers. Hence, such prototyping platforms must include reprogrammable devices to offer a wide exploration space. These kinds of devices include CPLDs, DSPs, FPGAs on the digital side and variable gain amplifiers, adjustable local oscillators, programmable filters for example in the analogue domain. In this context, the design of the mixed platform described here is mainly based on previous work carried out in the Institute dealing with the design of programmable RF transmit and receive boards [2]. A direct-conversion architecture (also known as zero-IF) was chosen for the following qualities: low power dissipation, large frequency tuning range, ease of design and low-cost associated with the reduced component count. Reconfigurability of the different elements is done using the serial I²C interface.

The complete system is composed of two RF modules (a transmit board and a receive board) and a digital bridge between them and a PC. The global objective of this Base-Band Board (hereafter called BBB) is to provide a flexible and efficient link between the existing RF front-ends (both transmit and receive) and digital signal processing executed by a PC. To achieve such a goal, data sent to or received from fast signal converters must be linked to a computer using a reliable and efficient interface. Moreover, it should allow some configurability to cope with different standards and enable some off-loading of the DSP functions from the PC to the BBB. Along with these requirements, the low-cost aspect led some of the choices described in the following section. The performance and design possibilities of the BBB are explored in the third paragraph and we will then discuss the opportunities created by this work.

2. TECHNICAL CHOICES

The three main capabilities of the BBB are presented in this section. First, the digital link enables sharing data and configuration information between the hardware and a PC. A/D and D/A converters send to and receive data from the RF blocks. Between these two modules, a digital device synchronizes the data flows and can possibly process the digital signals.

2.1. Hardware to PC communication

2.1.1. Data transfers

Among the wide variety of standards available, USB was selected because of its ease of use, availability on most of PCs, and accessibility (specifications and drivers are downloadable free of charge leading a large community to use USB).

The USB PHY chip chosen is the CY7C68013A [3], integrating in a single chip a USB2.0 transceiver (with High-Speed 480 Mbps capability), a serial-interface engine (SIE), an enhanced 8051 microcontroller and a programmable peripheral interface, thus giving the desired

flexibility. The 128-pin version of this chip offers a General Programmable InterFace (GPIF) which is a customizable 16-bit bidirectional parallel port. Its behavior is controlled by state machines (also called waveforms) defining the behavior of up to 6 control (CTL, output-only) and 6 ready (RDY, input-only) signals.

2.1.2. Configuration data

The CY7C68013A has an integrated I²C master-only controller which runs at 100 or 400 kHz. Via this interface, the 8051 can control peripherals using both I2CTL and I2DAT specific registers. This functionality is used to configure the RF elements from the PC through the I²C port.

2.2. Digital base-band to RF section interface

The requirements of the data converters have been extracted from previous studies [4]. For the resolution, 8 to 18-bit converters are required according to the standard used. The sampling rate, since zero-IF architecture is used, simply has to fulfill Nyquist's criterion, that is to say that it has to be at least twice the bandwidth of the digitized channel.

The ADCs selected are from the LTC220x series from Linear Technology [5]. Their 16-bit resolution gives 8 bits of dynamic range to allow amplitude variation of the incoming signals for the least demanding standards. This ADC series can operate from 10 to 250 Msps, sharing the same footprint (Table 1). This means that the speed can be selected according to the bandwidth of the standards to be handled by the prototype. Nevertheless, the power supply for these devices should be carefully chosen since the consumption increases dramatically with the sampling frequency.

Table 1. LTC220x series performances.

ADC type	Sampling rate (Msps)	SNR (dB)	Consumption (mW)
2202	10	81.6	140
2203	25	81.6	220
2204	40	79.1	480
2205	65	79.0	610
2206	80	77.9	725
2207	105	77.9	900
2208	125/135	77.7	1250
2209	210/250	77.1	1450

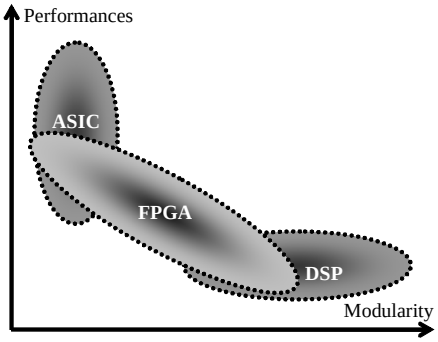
The DAC is a dual 16-bit 200Msps MAX5875 from Maxim Integrated Products [6]. This specification is sufficient even for GSM 1800, the most demanding standard considered here.

The 64-pin package ADCs and the 84-pin package dual DAC keep pin count low which greatly simplifies the final PCB layout.

2.3. Digital base-band processing

The core of the BBB is the device dealing with synchronization of incoming and outgoing data flows. An overview of the different possibilities, sketched on Figure 1 indicates that, for our application, an FPGA offers the best combination of performance and modularity, enabling customization, sufficient pin count, with a wide range of specification to cost ratio compared to the other devices [7]. Its use in software radio has become common nowadays [8].

Figure 1. Trade-off between the main digital device families.



This FPGA has to fulfill three different tasks. First, it interfaces with the 4 converters, directly providing them a reconfigurable clock. It also communicates with the PHY chip in order to achieve fast data rates, transmit configuration parameters to the converters and RF blocks and report the status of the different parts of the system. Finally, hardware functions and reconfigurable digital processing can be efficiently implemented. For example, it provides the possibility to increase the overall bandwidth of the system by implementing an upsampling stage with the use of root raised-cosine filtering.

The pin count proposed in Table 2 suggests the use of a minimum of 122 I/Os on this device.

Table 2. FPGA pin count.

IOs	Number of pins	Purpose
ADCs	32 data + 6 ctrl	Data conversion
Double DAC	32 data + 2 ctrl	Data conversion
Ports A, B & D	27	Data transfer
RDY & CTL	12	Protocol
I²C	2	Configuration
JTAG	7	FPGA initialization
clocks	2	50MHz + USB
total	122	

A Xilinx Spartan3E 250 or 500 kgates FPGA (Table 3) in a 208 pin package offers sufficient performance while limiting the pin-count and the complexity of the layout

design along with the cost of the prototype [9]. The unused 24 pins (dual purpose configuration pins are not used to carry other signals) are directly mapped to a general purpose expansion port which can be used to interface with the user (LEDs, pushbuttons, display…) or other systems (RS232 port, VGA interface, audio codec, etc…).

Table 3. Spartan 3E 250 and 500 main features.

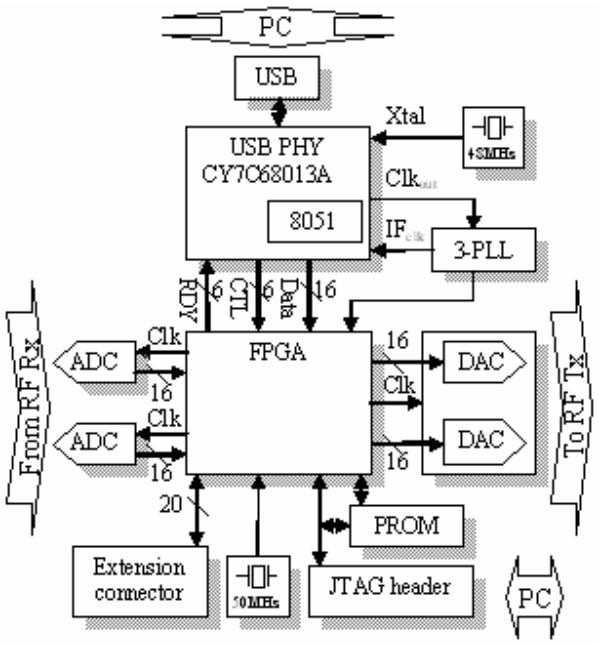
Device	XC3S250E	XC3S500E
System Gates	250K	500K
Equivalent Logic Cells	5,508	10,476
Distributed RAM	38Kbits	73Kbits
Block RAM bits	216K	360K
Dedicated Multipliers	12	20
DCMs	4	4

3. IMPLEMENTATION

3.1. Hardware

Figure 2 summarizes the different elements implemented on the BBB.

Figure 2. Synoptic view of the BBB.



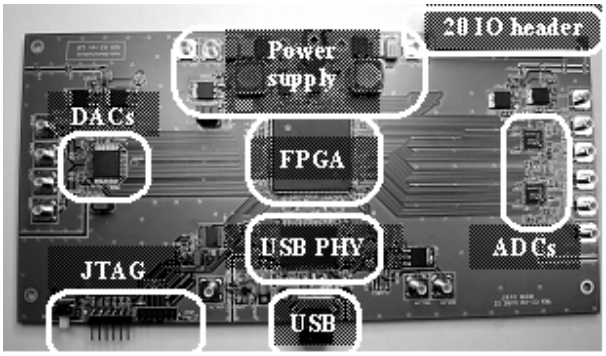
The use of an PFGA together with intelligent I/O pin assignment considerably simplified the PCB layout. The final PCB had four layers: layer 1 (top) is primarily a signal layer, layer 2 is for grounding, layer 3 for power supply distribution and layer 4 for low-speed signals and power distribution. Noise and interference sensitive sections such as the ADC, DAC and USB have separate ground planes which are connected to the main ground using ferrite PI filter.

Four kinds of connectors are available: USB, JTAG, a 40-pin IDC header and SMBs. The SMBs have different purposes and are used to connect the BBB and the RF Rx and Tx modules. They are placed so as to match the footprint of the boards. 8 SMB connectors are used for the differential access to the 4 data converters, 4 carry the I²C signals (clock and data) separately to the Rx and Tx RF boards and 2 are 7 volt power supply connections. The 2 power supply connectors enable both the RF boqrds qnd the BBB to be powered using a single power adapter.

An EEPROM linked to the FPGA, selectable with a jumper, can host a configuration bit stream. If it is pre-programmed, the board can be used as a standalone system and does not require a computer.

The final PCB, shown on Figure 3, is 210 x 105mm.

Figure 3. Picture of the final BBB.

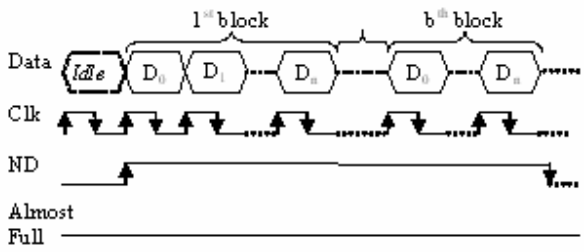


3.2. Firmware

As mentioned previously, the FPGA has to synchronize data streams between the data converters and the USB interface. To do so, the customizable 16-bit GPIF of the PHY chip is used and FIFOs are instantiated on the FPGA. To be sure that there is no loss of data, one must ensure that Tx and Rx data rates are always slower than the GPIF interface. The asynchronous FIFOs, are based on a custom VHDL model. Its special features are: generic data size, generic depth and generic “almost full” and “almost empty” levels. This last option enables adjusting the behavior of the FIFO to the requirements of the GPIF and the specificities of the USB driver [10]. Since the data is organised in blocks of a predetermined size, the “almost full level” can be set, for the Tx side, one block lower than the last data address in the FIFO. Then it prevents the FIFO from overflowing and ensures the integrity of the data. Considering the use of block RAM only, the memory available on the FPGA (Table 3) is equivalent to 13.5 or 22.5 ksamples of 16 bits.

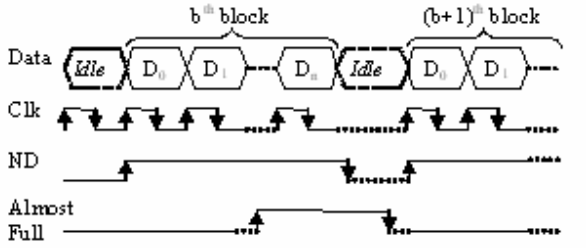
During normal USB writing operation (Figure 4), blocks are stored in the FIFO as long as ND (one of the GPIF CTL signals) is asserted.

Figure 4. Data written by the GPIF, normal operation



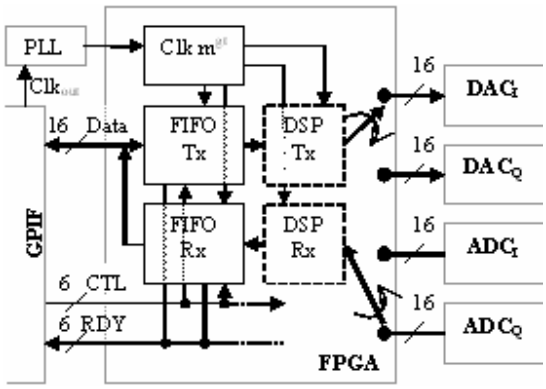
If the FIFO is about to overflow (Figure 5), the almost full flag is active and mapped to one of the GPIF CTL signals.

Figure 5. Data written by the GPIF, interruption by the application



The data rates achieved using this scheme are for a unidirectional connection is 262 Mbps, in theory, the same rate will be obtained for a bidirectional connection. This figure is to be compared with the theoretical maximum data rate announced on the USB documentation. Further details can be found in [10]. The USB data rate is lower than the throughput of the converters. Indeed, assuming that the converters are clocked at 100 MHz, a one-way I/Q transmission is equivalent to 3.2 Gbps. One way to optimize the design with these two different data rates is to implement digital signal processing on the FPGA using distributed logic and multiplier blocks. These processing can have two purposes: they can increase the overall bandwidth of the system with multirate filtering and they can off-load some DSP functions from the PC to the board (Figure 6). Both objectives can be fulfilled with the use of a multirate FIR filter (such as the polyphase architecture) having a root raised-cosine transfer function. Thus, hardware extraction of the information for reception (filtering and decimation) and shaping for transmission (filtering and interpolation) can dramatically reduce the stress on the BBB to PC connexion. Other architectures, using more complex sample rate conversion schemes can be found in [11].

Figure 6. FPGA content.



4. DESIGN POSSIBILITIES AND FUTURE WORK

Among the various possibilities offered by this system, implementation of soft-core processors on the FPGA is of interest for future developments. Spartan 3 FPGAs can benefit from the use of the XPS environment [7] to implement, size and program the Microblaze RISC architecture. Other soft core embedded microcontroller like 8051 [12] can be implemented and the software can be changed on the fly with partial reconfiguration of the block RAM. Their purpose on our system would be to compute algorithms such as timing recovery and carrier recovery to reduce the load on the BBB to PC connection.

5. CONCLUSION

A low-cost design of a mixed-signal platform has been presented. Its capabilities and performances have been discussed and demonstrate sufficient flexibility and reliability for exploration and experimentation in software defined radio. It has also proven better specification in terms of computational resources, resolution and data rates compared to other present low-cost prototyping systems available [8].

This platform has been fully validated. Connection with the RF modules has been tested and further experimental results will be provided during the conference.

The next generation of BBB is planned and should allow enhanced performance with the use of a faster communication standard than USB (such as Serial ATA), and an FPGA with more logic resources and functionality, optimized for fast signal processing.

6. AKNOWLEDGEMENTS

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