ON THE ACCURACY AND HARDWARE REQUIREMENTS OF CORDIC BASED PHASED ARRAY CALIBRATION

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Where an array of separate transceivers has a requirement for coherent combination of transceived signals, it is necessary to address the 'calibration problem' [1]. Having previously considered this problem in the context of a tower-top, cellular, transmitter and - given the conflicting requirements of reliability, cost, scalability and performance - the solution shown in figure 1 was proposed [2]. This system may be scaled to an array of any size by repeating this tessellating structure.



Figure 1. The tower-top calibration system.

It can be shown that the calibration accuracy of this system is limited by i) the balance of the electromagnetic coupler structure and ii) sensor measurement accuracy [2]. Thus, given an electromagnetic coupler with RMS error of, $\Phi_c = 1.117^\circ$ and $\delta_c = 0.3295 \text{ dB}$ [3], the total error contribution (ϵ_c) to the RMS sidelobe level for a 25 element array is shown in figure 2. A -35 dB RMS sidelobe level specification is derived, limiting the total measurement error contribution to the shaded area of figure 2.

We present the design method for a CORDIC [5] based transmit (and by reciprocity receive) calibration process for M-ary signals to meet an RMS sidelobe specification.



Figure 2. The array calibration error due to coupler imbalance, for a 25-element array and its effect on RMS sidelobe level. The shaded area represents permissible additional sidelobe increase due to measurement error.



Figure 3. Calibration measurement and control scheme

Figure 3 illustrates the basic calibration system; this corresponds to the sensor and controller blocks of figure 1. Three CORDIC blocks are used to effect QPSK calibration, vector mode CORDIC measures the transmitter output, then rotation mode CORDIC (after additional processing) applies the calibration. The second vector mode CORDIC allows a phase offset to the input baseband transmit signal, permitting beamforming.



Figure 4. The impact of reduced input magnitude on vector mode CORDIC accuracy.

The accuracy of the vector mode CORDIC block is shown as a function of ADC code offset (up to 15 bits) in figure 4. We derive formalism showing that after three calibration cycles, due to noise and overshoot, that 50% of the ADC resolution (M) is accessible. Moreover, that for a given sidelobe level (σ^2) the required ADC resolution is given by:

$$M - 1 = \log_2\left(\frac{1}{1.2\delta_m}\right) \tag{1}$$

where:

$$\delta_{m} = \frac{1}{(5c+1)} \left[-c\Phi_{c} + \delta_{c} \pm \sqrt{\Phi_{c}^{2} + 2c\Phi_{c}\delta_{c} - 5c\delta_{c}^{2} + (5c+1)N\overline{\sigma}^{2}} \right]$$
 2)

Where N = the number array of elements, c = 5.68 for CORDIC and α is a constant, dependent upon both the calibration algorithm and array size employed. A graph of equation 1 (see figure 5) shows that our specification is met by M = 10 bits, however, increased calibration accuracy is accessible through higher ADC resolution.



Figure 5. Predicted and simulated (a = 1.66, c = 5.68) ADC resolution results for N = 25.

Synthesis for a VIRTEXII PRO-XC2VP30 target FPGA [6] demonstrates operation up to 130 MHz using only 2488 slices (18%). Results from these simulations, also shown in figure 5, validate our theoretical predictions.

References:

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