Undersampling Observation-Based Compact Digital Predistortion for Single-Chain Multiband and Wideband Direct-to-RF Transmitter

Article *in* IEEE Transactions on Microwave Theory and Techniques · October 2017

DOI: 10.1109/TMTT.2017.2758366

CITATIONS
6

READS
276

3 authors, including:

Ziming Wang
National University of Ireland, Maynooth
9 PUBLICATIONS **18** CITATIONS

SEE PROFILE

Lei Guan
Nokia
28 PUBLICATIONS **641** CITATIONS

SEE PROFILE

Undersampling Observation-Based Compact Digital Predistortion for Single-Chain Multiband and Wideband Direct-to-RF Transmitter

Ziming Wang, *Graduate Student Member, IEEE*, Lei Guan, *Member, IEEE*, and Ronan Farrell, *Member, IEEE*

***Abstract*— Modern wireless network operators are consistently looking for improvements in the wireless access infrastructure that minimize size, weight, and power. Therefore, compact multiband RF and wideband RF solutions offer an attractive role in forthcoming fifth generation networks. This paper presents a novel compact wideband RF transmitter architecture that is based upon an undersampled digital predistortion (DPD) methodology. The proposed architecture minimizes the required number of RF/analog components in the system by using RF-DAC-based direct RF sampling at the forward transmitter data path and one undersampled analog-to-digital conversion (ADC) with certain bandpass filters at the DPD sampling receiver path. Extensive experimental results validate that the DPD-enabled RF transmitter bandwidth can be significantly increased using the proposed multirate track-and-hold amplifiers architecture. Experimental tests achieved multiple GHz DPD bandwidths with satisfactory linearization performance via very compact sampling receiver that has one undersampled ADC. Particularly, we evaluated three application scenarios: 1) three-band carrier aggregated LTE signals (each one occupying 20-MHz instantaneous bandwidth), the linearization performance achieved 50-dBc adjacent channel power ratio (ACPR) with more than 1-GHz bandwidth using ADC running at 76.8 and 61.44 MSPS; 2) single-band LTE signal with continuous 100-MHz instantaneous bandwidth, the linearization performance achieved −48-dBc ACPR using 61.44-MSPS ADC; and 3) single-band LTE signal with continuous 20-MHz bandwidth at 4 GHz, the linearization performance achieved −54-dBc ACPR using 61.44-MSPS ADC.**

***Index Terms*— Digital predistortion (DPD), multiband transmitter, power amplifier (PA) linearization, RF-DAC, undersampling analog-to-digital conversion (ADC).**

I. Introduction

WIRELESS communication networks are evolving rapidly. Fast expansion of consumer demand for better service experience is calling for the fifth generation (5G) higher data-rate wireless access technologies. Given the variances in spectrum regulation in different countries, it is tough for one operator to obtain a continuous wideband frequency spectrum (especially under 6 GHz), leaving frequency fragments situation in general. There are several important initiatives in the improvement of the wireless access network performance. The first option is to consider new frequency bands, for example, higher frequency bands, particularly millimeter wave bands. Alternatively, this can be achieved by architectural innovations. One example is the consideration of a large-scale antenna system that will significantly increase the spectrum utilization efficiency at the cost of massive RF digital signal processing horsepower [1], [2]. A second approach is to develop a flexible multiband carrier aggregation-type wireless system that will use multiple frequency bands simultaneously to create a single visualized and aggregated wider frequency band for the wireless access network. This paper presents an efficient architecture that supporting this latter approach.

The emerging RF-class data convertor, e.g., RF-DAC, enables an appealing single-chain multiband (or wideband) transmitter architecture. However, to boost the RF power conversion efficiency delivered by the multiband (or wideband) power amplifiers (PAs) and to maintain reasonable signal quality (linearity), we still require high-performance PA modules and multiband (or wideband) RF signal conditioning modules [3], [4], such as multiband (or wideband) digital predistortion (DPD) units.

As shown in Fig. 1, the conventional transmitter architecture, using DPD, requires multiple forward data paths and multiple feedback paths. The complexity of providing sufficient linearization performance over multiple nonadjacent bands requires a DPD estimation algorithm with a dramatically increased number of coefficients than for a single-band system, such as common 2-D-DPD approach and its variations [5]–[8]. Those multidimensional approaches increase the computational overhead for utilizing DPD-based systems in multiband transceivers. For the sake of reducing the complexity of the concurrent multiband DPD systems, recent works have tried to either reduce the sampling rate at each of the feedback paths [9] or limit the feedback path bandwidth by certain band-limited functions [10], [11] or decrease the number of the feedback paths [12].

Previously in [13], we outlined and presented a compact single-chain multiband DPD solution using only one undersampling analog-to-digital conversion (ADC) and a low-pass filter to replace the conventional multiple DPD feedback paths. We generalized this new architecture as shown in Fig. 2. Previous work demonstrated that a modified DPD scheme with a single ADC at 76.8-MSPS sampling rate achieved

Manuscript received June 30, 2017; revised September 13, 2017; accepted September 19, 2017. This was supported in part by the Science Foundation Ireland and in part by the European Regional Development Fund under Grant 13/RC/2077. *(Corresponding author: Ziming Wang.)*

Z. Wang and R. Farrell are with the Department of Electronic Engineering, National University of Ireland Maynooth, Maynooth, Ireland (e-mail: ziming.wang666@gmail.com).

L. Guan is with Innovation Incubation, Nokia Bell Labs, D15 Y6NT Dublin, Ireland (e-mail: lei.guan@nokia-bell-labs.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2017.2758366

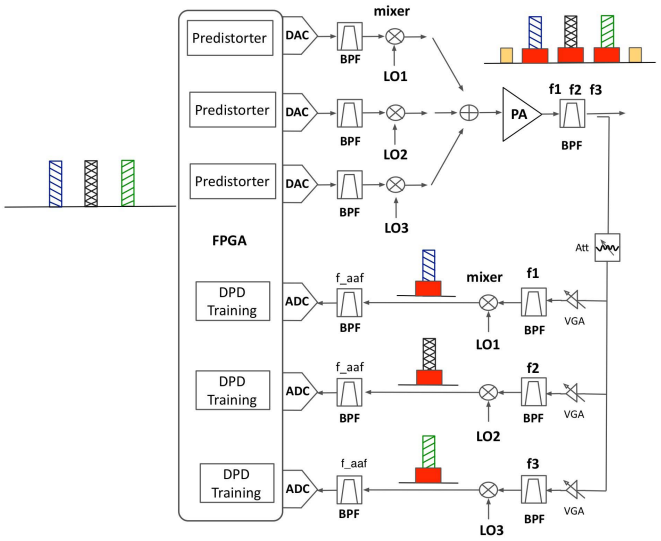


Fig. 1. Simplified diagram of a conventional DPD-enabled concurrent multiband wireless transmitter.

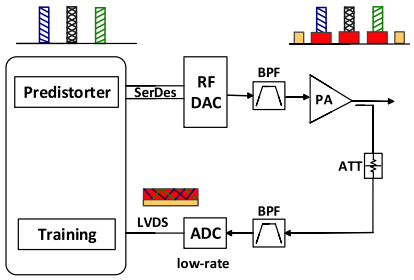


Fig. 2. Simplified diagram of the single-chain DPD system.

satisfactory linearization performance for triple-band LTE-A applications (20-MHz bandwidth each), i.e., −55-dBc adjacent channel power ratio (ACPR) for 1-GHz RF bandwidth.

In this paper, we further extend the previous work from the following critical perspectives: 1) an investigation of the essential limitation parameters of the proposed architecture, especially, the limitations on maximum achievable bandwidth at the DPD sampling receiver path due to the utilization of one single-input ADC; 2) the extension of the DPD sampling receiver bandwidth to wider bandwidths by properly addressing certain essential parameters of ADC; and 3) to further validate the concept with both wideband singe-band LTE and multiband LTE signals.

This paper is organized as follows. In Section II, we revisit the undersampling DPD approach regarding basic system architecture and DPD processing basis. Then, in Section III, we present an advanced compact DPD solution using the wideband undersampled ADC-based DPD sampling receiver architecture. In Section IV, we perform a system-level analysis of the proposed architecture and lay out the corresponding practical concerns. Section V validates the proposed approaches via experimental tests, and then, we conclude this paper in Section VI.

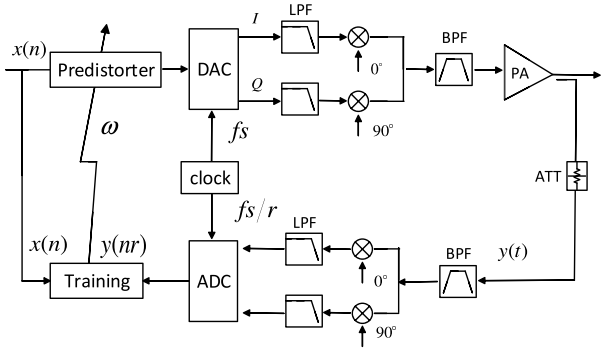


Fig. 3. Simplified diagram of the single-chain DPD system.

II. Undersampling DPD Basis

A generalized DPD comprises of a time-series-based behavioral model and least square (LS)-type (or its wider range derivatives) DPD parameter estimation algorithm. Particularly, this estimation can be performed by using feedback samples collected at any sampling rate as long as the ADC input bandwidth is sufficient to cover the whole observation band [14], and the captured data sequence can represent the statistical properties of the signals [15].

Previously, we initialized a DPD technique using the low-rate aliased feedback samples [13], [14]. Fig. 3 captures the simplified diagram of the undersampling DPD introduced in [14], and it includes a data forward path with predistorter function at high data rate and a feedback path with undersampling function at low data rate. The DPD coefficients were estimated using the high-rate input signal and the aliased low-rate feedback signal under the direct learning structure. The low-rate I/Q feedback samples are captured by a dual-input low-rate ADC after an I/Q demodulator in the feedback path, the r is the reduction ratio of the sampling rate of the feedback ADC. It is worth noting that the antialiasing filter preceding the low-rate ADC is the same as the filter for the high-rate DAC, which is usually 3–5 times signal bandwidth to guarantee the accuracy of the analog input signal of ADC.

In principle, any valid linear-in-parameter polynomial type of behavioral models can be integrated in the DPD system. For simplicity, in this paper, we will use the generalized memory polynomial (GMP) model basis as follows:

$$\phi_n^m = \sum_{l\in L}\sum_{p\in P} x(n-l)|\,x(n-l)\,|^p$$
$$m = P \times L \tag{1}$$

where P and L indicate the nonlinear order and the memory depth, respectively, and m is the number of the coefficients.

The predistorted signal (pd) can be obtained by

$$pd(n) = \phi_n^m \cdot \omega. \tag{2}$$

The coefficients can then be estimated using the LS algorithm as in (3)–(6)

$$e(nr) = x(nr) - y(nr) \tag{3}$$
$$\phi_{nr}^m \cdot \omega_e = e(nr) \tag{4}$$
$$\omega = \omega + \omega_e. \tag{5}$$

Equation (4) is the multirate overdetermined equation, which is high rate in row and low rate in column. The matrix form of (4) can be written as

$$\begin{bmatrix} \phi_{0,0} & \phi_{0,1} & \cdots & \phi_{0,m-1} \\ \phi_{r,0} & \phi_{r,1} & \cdots & \phi_{r,m-1} \\ \vdots & \vdots & \ddots & \vdots \\ \phi_{nr-1,0} & \phi_{nr-1,1} & \cdots & \phi_{nr-1,m-1} \end{bmatrix} \times \begin{bmatrix} \omega_0 \\ \vdots \\ \omega_{m-1} \end{bmatrix} = \begin{bmatrix} e_0 \\ e_r \\ \vdots \\ e_{nr-1} \end{bmatrix}. \quad (6)$$

Then, the coefficients are obtained from the determined equation constructed according to the LS algorithm

$$\left(\phi_n^{mT}\phi_n^m\right) \cdot \omega_e = \phi_n^{mT} \cdot e(nr). \quad (7)$$

As proposed in [14], the determined equation obtained by LS can be treated as the combination of autocorrelation matrix and cross-correlation matrix, as shown in

$$R_{\phi\phi} = E[\phi^T \phi] \quad (8)$$

$$R_{\phi y} = E[\phi^T y] \quad (9)$$

where $R_{\phi\phi}$ is the autocorrelation matrix and $R_{\phi y}$ is the cross-correlation matrix. Moreover, we have

$$R_{\phi\phi} = \int \phi^T \phi \cdot \rho(\phi) d\phi \quad (10)$$

$$R_{\phi y} = \iint \phi^T y \cdot \rho(\phi, y) d\phi dy \quad (11)$$

where $\rho(\phi)$ and $\rho(\phi, y_n)$ are the probability distribution function and the joint probability distribution, respectively.

In (3), the error samples are calculated from aligned low-rate feedback samples and low-rate input samples. In the training process, the multirate behavioral model is constructed using high-rate input signal. According to (10), given a behavioral model, the cross-correlation matrix is determined by the accuracy of the feedback sample value and the accuracy of the joint probability function $\rho(\phi, y_n)$, which is the information carried by training samples. Given the sufficient number of samples, the information carried by the low-rate modulated signal can be self-reserved by the cyclostationary property. Thus, it only requires the accuracy of captured samples in the feedback path design, and the aliasing effect in frequency domain will not distort the coefficients estimation using LS. Furthermore, to guarantee the accuracy of the magnitude value (not statistical property) of captured low-rate samples, the analog input of ADC must not be aliased in the analog domain, simply because the aliased analog input of ADC will affect the value of the samples that are converted to the digital domain. Therefore, the antialiasing filter proceeding the low-rate ADC should be the same as the filter for the high-rate DAC, for sure, it is not necessarily 3–5 times of signal bandwidth, and it depends on the required linearization bandwidth at the forward path in the system.

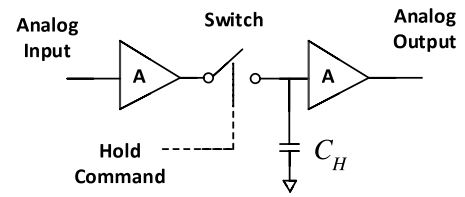


Fig. 4. Basic open-loop THA consisting of a switch, hold capacitor, and input and output buffers.

III. Advanced Compact Single-Chain DPD System

This section introduces an advanced compact single-chain DPD system. We will address the challenges from hardware and algorithmic perspectives, respectively.

A. System Hardware Architecture Overview

Let us recall the proposed compact DPD system as shown in Fig. 2. In this architecture, we intentionally remove the discrete components-based intermediate frequency (IF) stage, including mixers, corresponding local oscillators (LOs), and anti-image filters stages in both the forward path and the feedback path. Simply, multiple concurrent baseband signals or continued wideband signals are processed in the digital domain and upconverted to the RF analog domain by RF-DAC. A single-input low conversion-speed undersampling ADC with a bandpass filter and the attenuator are employed to replace the entire observation path. To guarantee the accuracy of the analog input of ADC, the bandwidth of the antialiasing filter and the sample-and-hold circuits of the ADC stay the same as the interested forward path system bandwidth. The sampling rate of ADC fs_{ADC} is fractional times the data forward path RF-DAC sampling rate fs_{DAC}.

B. Extending the Observation Bandwidth by Multirate Track-and-Hold Amplifiers

Theoretically, undersampling DPD can be performed using feedback samples collected at any sampling rate. In practice, the maximum observation bandwidth and the minimal sampling rate of feedback path are determined by the equivalent capture bandwidth of the track-and-hold amplifier (THA), preceding the ADC which is shown in Fig. 4. The THAs function is to sample the input signal at a precise instant and hold the value of the sample constant during the ADC process. There are two modes of operation in a THA. In the track mode, the voltage on C_H is adjusted to the real-time voltage level at the analog input by charging and discharging the capacitor. During the hold mode, the hold capacitor C_H is disconnected from the input buffer and is expected to retain the voltage present prior to the disconnection. The droop rate, as shown in Fig. 5, is the rate that the output voltage is changing due to leakage from the hold capacitor. This combination of acquisition and droop determines the veracity of the captured sample but places opposing constraints on the capacitor C_H. By increasing the value of C_H, it increases the effective hold period but reduces the input bandwidth at the same time. Thus,

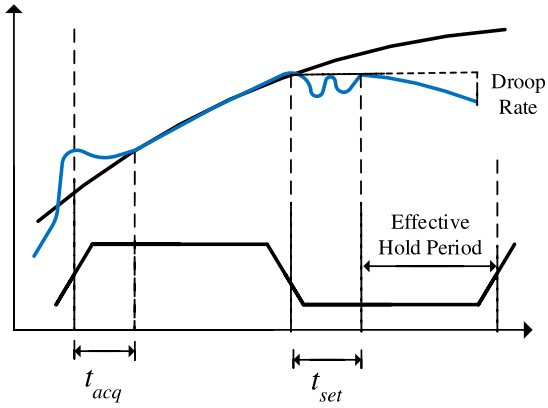


Fig. 5. Common operation for THA.

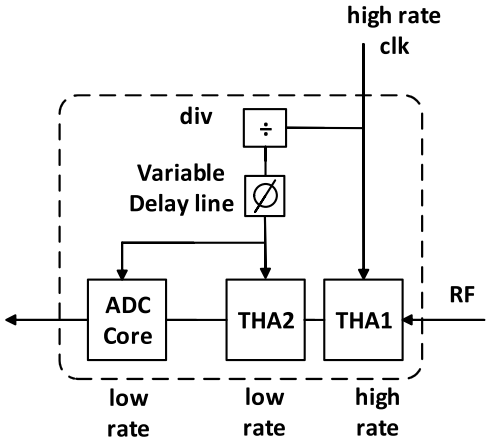


Fig. 6. Proposed undersampling ADC with multirate THA circuits.

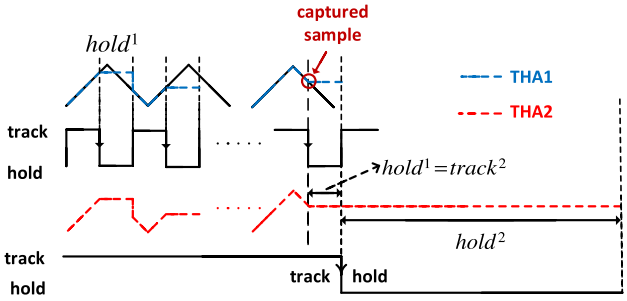


Fig. 7. Timing diagram of the multirate THA circuit.

it is not practical to achieve lower sampling rate and higher input bandwidth using a single THA.

To extend the analog bandwidth of the ADC, we proposed an undersampling ADC consisting of the multirate THAs and a low-rate ADC core as shown in Fig. 6. The multirate THA circuit is consisted of a high-rate THA1 with wide input bandwidth and a low-rate THA2 with long hold period. The THA1 holds a captured sample value, which is tracked and held by THA2. Fig. 7 shows the timing diagram of the multirate THAs. The output of the hold mode can be treated as a dc signal. So as for the THA2, it is employed to track and hold a short dc signal from the THA1. The long acquisition

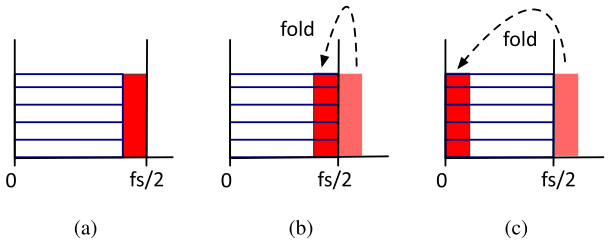


Fig. 8. (a) High-rate original complex samples. (b) Aliased low-rate real-number samples. (c) Aliased low-rate complex samples.

period from the low-rate THA2 happens at the begin of track mode, which will not affect the actual captured sample at the end of track mode of THA2 (track^2). The input clock of the undersampling ADC is the high-rate clock for the THA1. It is divided and delayed to a low-rate clock for the THA2 and the ADC core. The sampling rate of the undersampling ADC is determined by the low-rate THA2. The capturing error of the entire system comes from both the high-rate THA and the low-rate THA. The synchronization of the THA1 and THA2 is critical in this design. Due to the variety of propagation delays and digital delays of multirate THAs, a delay line is employed to compensate the timing.

C. DPD Training Using Real-Number Feedback Samples

Usually, in a DPD system, analog demodulation or digital demodulation is required to obtain the in-phase and quadrature (IQ) components at the feedback path. In the proposed compact DPD system, the undersampling ADC directly captures the RF feedback signal. As the IF stage (analog demodulator) is eliminated, the captured sample value is real number, which introduces two processing challenges.

The first challenge is the different aliasing schemes of complex signals (baseband) and real-number signals (analog). In brief, Fig. 8 shows the difference between the aliased baseband complex signal and the aliased analog real-number signal. To calculate the coefficients of DPD in the direct learning structure, the errors of the low-rate original samples and the related low-rate feedback samples are necessary, as shown in (3). However, the demodulated IQ samples from the captured low-rate real-number feedback samples are not corresponding to the low-rate original IQ samples, as shown in Fig. 8.

The other challenge using the aliased feedback samples without the analog demodulator is the high-order anti-image filter required in the generalized undersampling DPD. In the undersampling DPD system, if the sampling rate of the single ADC is lower than the half of the signal bandwidth, the spectrum of aliased feedback samples will fully fill the Nyquist zone. To eliminate the modulation image in this case, the order of the anti-image filter will be considerably high.

Chani-Cahuana *et al.* [16] proved that only the acquisition of either I or Q component of the feedback signal is required for the DPD training. The feedback samples without the phase information can be used to estimate the coefficients. So, to address those two challenges mentioned earlier, the

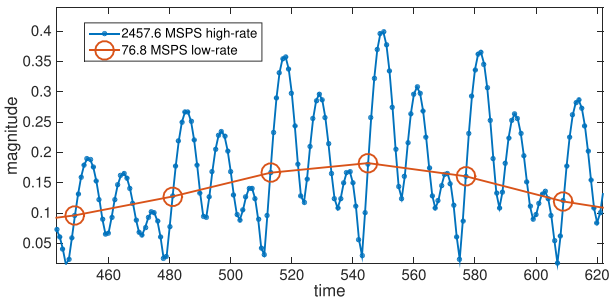


Fig. 9. Example of time-aligned multirate training samples.

RF signal without demodulation is used to calculate the error function in the proposed DPD training procedure, which avoids two issues mentioned earlier.

To calculate the real-number error, the original baseband complex samples are first modulated to the real-number samples $\bar{x}(n)$. Then, a multirate time alignment scheme is employed to align the PA input samples and undersampled feedback samples. Without the loss of generalities, let us assume that the sampling rate of RF-DAC is r times the sampling rate of ADC at the feedback path. $\bar{x}(n)$ and $\bar{y}(n)$ represent the real-number high-rate input and feedback samples, respectively. Then, the captured feedback samples by the undersampled ADC can be represented as $\bar{y}(nr)$. The original high-rate input signal can be downsampled to produce a low-rate input signal with the same time resolution as the low-rate feedback signal. By introducing different phase shifts (0 to $r-1$) in the downsampling processing, we will have r sets of low-rate input signals that can be utilized to perform cross-correlation-based time alignment. The ith ($i \in [0, r-1]$) correlation result that has the largest peak value indicates that the input downsampled subset x_{in} will be used for time alignment. Then, the second time alignment was carried out by cross correction between $\bar{x}(nr+i)$ and $\bar{y}(nr)$. The time-aligned high-rate input and low-rate feedback are shown in Fig. 9.

Next, the error function used in the direct learning structure is constructed in

$$\bar{e}(nr) = \bar{x}(nr) - \bar{y}(nr) \tag{12}$$

where $\bar{x}(nr)$ and $\bar{y}(nr)$ are the real-number samples.

As the delay is calculated by the multirate time alignment method, the delay and the phase are compensated to the original complex signal to obtain the multirate behavioral model ϕ_n^m. Then, the overdetermined equation using real-number error is obtained in (13) according to [16]

$$M\omega_e = \bar{e}(nr) \tag{13}$$

where $M = [(\phi_{nr}^m)_I - (\phi_{nr}^m)_Q]$, ϕ_{nr}^m is the multirate behavioral model building by the high-rate complex input signal $x(n)$, the subscript I indicates the in-phase component, and the subscript Q indicates the quadrature component. The coefficients finally can be obtained using the LS algorithm as

$$\omega_e = (M^T M)^{-1} M^T \bar{e}(nr). \tag{14}$$

IV. System Analysis and Practical Concerns

A. System Analysis

In this section, we will discuss the proposed approach from system perspective including: 1) noise performance consideration at the analog chain; 2) power performance consideration at the DPD sampling receiver; and 3) DPD model coefficients estimation complexity.

In a conventional DPD-enabled multiband RF transmitter, the overall system noise performance of both data forward and feedback paths is typically dominated by the noise introduced by the frequency associated active analog components, such as PAs and RF-IF conversion stages. At the data forward path, the direct digital-to-RF architecture, particularly, RF-DAC devices, can be considered as one of the promising technologies to minimize the analog noise by eliminating the discrete components-based IF stage. Similar concept can be applied to the data feedback path, i.e., using direct RF-to-digital architecture, such as RF-ADC, at certain larger amount of the financial cost compared with the utilization of middle range ADCs together with analog downconversion stage solution (either low-IF or direct downconversion receiver architecture). The proposed compact approach not only eliminates the IF stage at the data forward path naturally by utilizing RF-DAC, but also removes the analog downconversion stage at the DPD feedback paths by using only one modified undersampling ADC.

Moreover, from power consumption perspective, the current RF-ADC architecture uses multiple converters inside the core, which increases the power consumption and introduces certain interleaving spurs. The proposed undersampling ADC architecture can achieve multi-GHz bandwidth as well. In contrast, as the undersampling ADC core operates at a low sampling rate, the proposed ADC structure consumes considerably less power without interleaving spurs. Utilization of the reduced sampling rate ADC architecture also eases the digital interface design between ADC chipsets and digital host chipsets, such as field-programmable gate array (FPGA) or DSP. For example, high-speed serial link (SerDes) interface used on RF-ADC will consume considerable high power per channel (150 mW running at 3.125 Gb/s), and power is also consumed while streaming the received packet into and out of the buffer memory [17]. In contrast, the LVDS-based digital interfaces, which can be used in the proposed undersampling ADC, will consume relatively low power per channel due to the significantly reduced amount of data to be transmitted.

Next, let us have a look at the DPD model complexity. The number of DPD model coefficients has been commonly utilized to describe the complexity of DPD model, and we follow the same concept here. A straightforward approach for performing multiband DPD is to build a multiple-input and multioutput DPD model, and the required number of DPD model coefficients increases significantly as the number of bands increases. This multidimensional expansion of the model coefficients will significantly increase the requirement of digital horsepower for DPD implementations. For example, 50 coefficients for a single-band DPD could grow to several hundred coefficients for a triband application [6], while

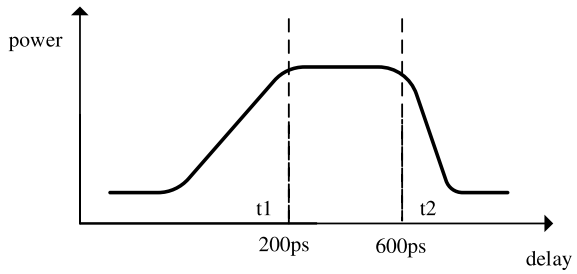


Fig. 10. Power of captured samples with different delays between the clock of THA1 and THA2.

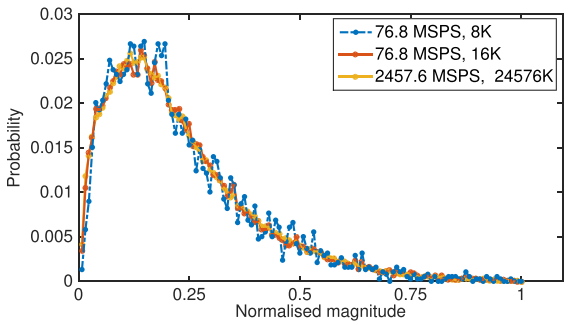


Fig. 11. Probability distribution with different numbers of training samples.

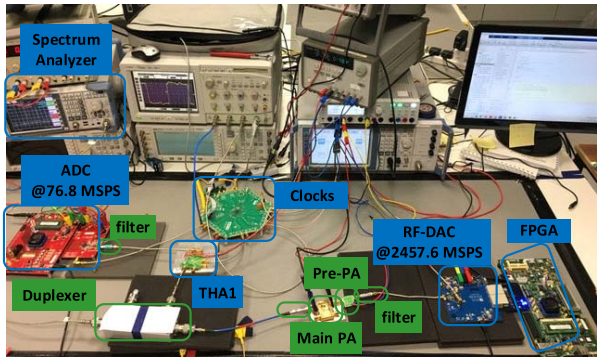


Fig. 12. Photograph of the test bench.

the proposed DPD architecture is naturally a single-input and single-output system, which architecturally minimizes the DPD complexity for multiband linearization applications. In other words, we achieved multiband DPD capability with considerably much lower single-band DPD complexity and power consumption. It is worth noting that, from DPD model perspective, our approach is very friendly and compatible with any linear-in-parameter models, such as GMP model [18], dynamic deviation reduction-based Volterra series models [19], MP model, band-limited model [10], and so on.

B. Practical Concerns

As we introduced a new design from both hardware and algorithm perspectives, it is worth mentioning some practical concerns for this compact DPD system.

In the multirate THA design, the synchronization of the THA1 and THA2 is critical. The relative delay between the clock of THA1 and THA2, which includes the propagation delays and the digital delays, can be calculated or observed by the oscilloscope offline. Nevertheless, a simple way to find the relative delay is to observe the power of captured samples. The multirate THA scheme can functionally work when the transition of the track mode to the hold mode of THA2 locates in the hold mode of THA1. Otherwise, the observation bandwidth is degraded. Thus, by observing the power of the captured samples with different relative delays, it is a simple matter to find the relative delay for synchronizing the multirate THA. As shown in Fig. 10, $t1$ indicates the transition from the track mode to the hold mode in THA1, and $t2$ indicates the transition from the hold mode to the track mode in THA1. The relative delay of the clock of THA1 and THA2 should be within $t1$ to $t2$.

The real-number original and feedback samples are used to calculate the error used in the direct learning structure. In the traditional DPD system, the phase (IQ rotation) between original signal and captured signal can be calculated as

$$p = (X^T Y)/(X^T X) \tag{15}$$

where X and Y are the $N \times 1$ vector of original and feedback complex-value samples, respectively. This phase (IQ rotation) value is compensated to the complex-value feedback samples in each iteration. In the proposed system, this phase should be calculated using a narrowband signal (no aliasing in captured signal) off-line and compensate as $1/p$ to the original complex-value original signal in the training process. Then, the complex-value original signal can be modulated to the real-number signal. Furthermore, the clocks generated for the RF-DAC and the undersampling ADC should be phase locked to guarantee the constant phase (IQ rotation) between the original signal and the feedback signal in each capturing.

The robustness of the proposed system is a practical challenge, because any interferences and unwanted spurs will be aliased into the feedback samples. The method, such as employing the forgetting factor in the recursive LS (RLS), is recommended to improve the robustness of the learning algorithm.

As analyzed in [14] and [15], the performance of the LS-based DPD coefficients extraction approach is largely determined by the probability information of the training samples. Furthermore, as for the modulated signals with cyclostationary properties (e.g., 4G LTE signals), the probability information is determined by the number of uniform-sampled data, rather than the sampling rate. Therefore, to properly carry out DPD coefficient estimation, we need a period of the training samples, the probability of which is close to the statistical properties of the actual transmitting signal. Fig. 11 shows an example of the probability function of a triband LTE signal, and 16k (16 384) low-rate training samples can be selected to extract the DPD coefficients robustly due to the statistical similarity (probability matching between training samples and transmitting samples).

V. Experimental Tests and Validation

A. Experimental Test-Bench Setup

To further validate the proposed compact DPD solution, an experimental test bed was assembled as shown

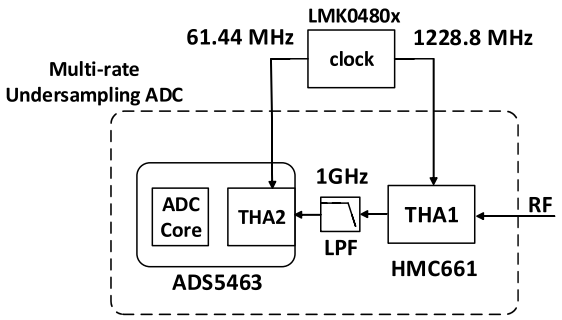


Fig. 13. Setup of the proposed undersampling ADC structure.

in Fig. 12. It includes an RF-DAC AD9129 with an FPGA board ML605 [20], ADC ADS5463 with a TSW1400 data capture board, a predriver PA HMC311SC70E, a main PA PAH-1+, a clock generator LMK04808, a wideband THA HMC661LC4B [21], bandpass filters, a low-pass filter, and a spectrum analyzer. The RF-DAC was running at 2.4576 GSPS. The ADC was running at 76.8 MSPS without THA1 for the test below 1 GHz. Then, it was running at 61.44 MSPS (30.72-MHz Nyquist bandwidth) with THA1 for the test above 1 GHz.

Furthermore, to verify the proposed undersampling ADC with multirate THA, the feedback path of the test bed was assembled following Fig. 13 for the tests above 1 GHz. The HMC661 ultrawideband THA was employed as the first rank THA (THA1) operating at 1.2288 GHz. This THA is claimed to provide maximum 6-GHz track-mode bandwidth with dc 18-GHz observation bandwidth. The second rank THA (THA2) is the THA inherent the ADC (ADS5463). A 1-GHz low-pass filter was placed at the output of the THA1 to optimize the signal-to-noise ratio by reducing the output amplifier noise contribution of THA1 [21]. The behavioral model used for all the tests was the MP model in (1). The RLS algorithm with 2^{-5} forgetting factor was used for the coefficients extraction. A 10-MHz LTE signal was used in calibration to calculate the phase and the delay. During each training procedure, the constant delay and phase values were compensated to the original input samples, rather than feedback samples.

B. DPD Performance Test Using Triband Carrier Aggregated LTE Signals (Under 1 GHz)

The first validation that we carried out was using triband carrier aggregated LTE signals with 11.7-dB peak-to-average power ratio. Each of component carrier has 20-MHz instantaneous baseband bandwidth) at the center frequencies of 710.4, 787.2, and 940.8 MHz, respectively. The RF-DAC was operated in a normal mode to generated RF signal at the first Nyquist zone (0–1.2288 GHz). The attenuated PA output signal was directly sampled by the ADC with a 1-GHz inherent sample-and-hold circuit. The 8k and 16k training samples were utilized to derive DPD coefficients. We implemented an MP model with the nonlinear order = 5 and memory length = 8 (40 coefficients in total). As shown in Fig. 14, the PA output spectra with and without proposed compact multiband DPD

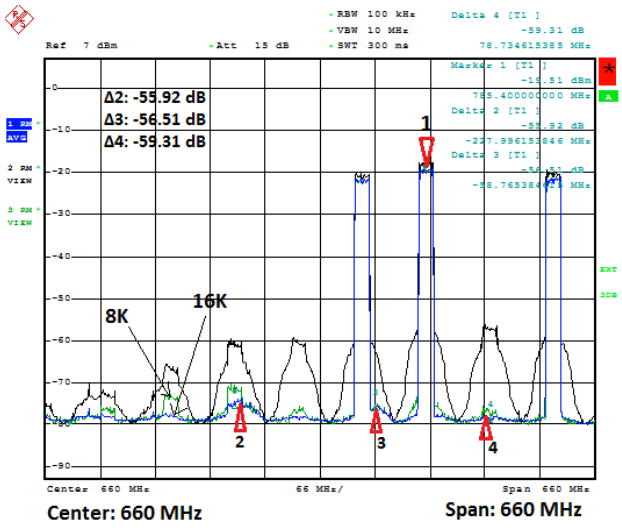


Fig. 14. Measured spectra of PA outputs before and after proposed DPD using triband LTE in 710.4, 787.2, and 940.8 MHz.

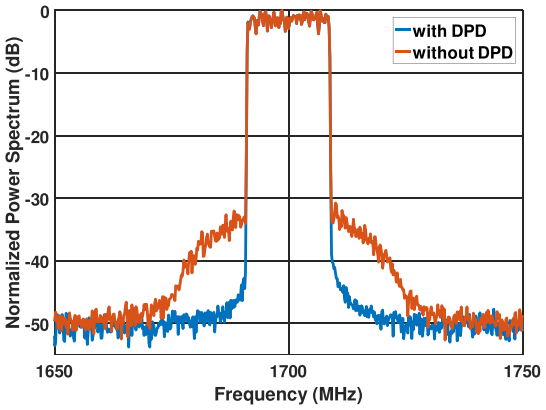
approach were captured by the spectrum analyzer. From the testing result, the ACPR performance can achieve below −55 dBc [13]. It is worth mentioning that, since the probability information of 8K samples of this triband LTE signal fluctuates around the accurate probability function of the long data set shown in Fig. 11, the ACPR performance using 8K samples degrades to some degree. The accuracy of DPD confirms to the accuracy of the probability information of the training samples.

C. DPD Performance Test Using Triband Carrier Aggregated LTE Signals (Above 1 GHz)

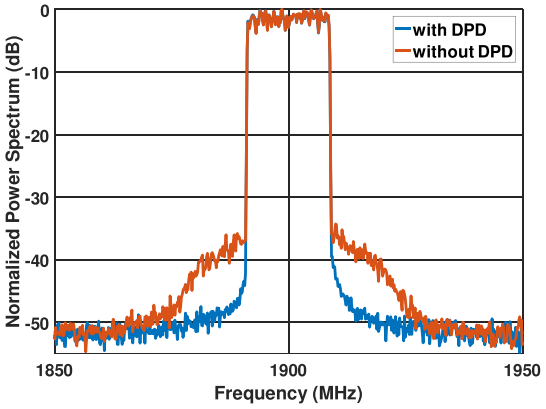
The second test was carried out using triband LTE signals at the center frequencies of 1700, 1900, and 2100 MHz, respectively. We utilized the same MP behavioral model with 40 coefficients. The RF-DAC was operated in mix mode to generate the RF signal at the second Nyquist zone (1.2288–2.4576 GHz). However, we found a considerable clock leakage in 2.4576 GHz, which folds back to the ADC Nyquist zone at dc in this mix mode. It decreases the dynamic range of the undersampling ADC due to the unwanted dc injection. The spectrum of PA outputs with and without DPD centering at 1700, 1900, and 2100 MHz is shown in Fig. 15(a)–(c), respectively. By utilizing the proposed compact DPD solution, the spectrum regrowth due to the PA nonlinearity and memory effects is eliminated, showing satisfactory multiband PA linearization performance. Furthermore, we captured small amount of the data to illustrate the AM–AM and AM–PM characterization performance, as shown in Fig. 16.

D. DPD Performance Test Using Continuous Wideband Signal

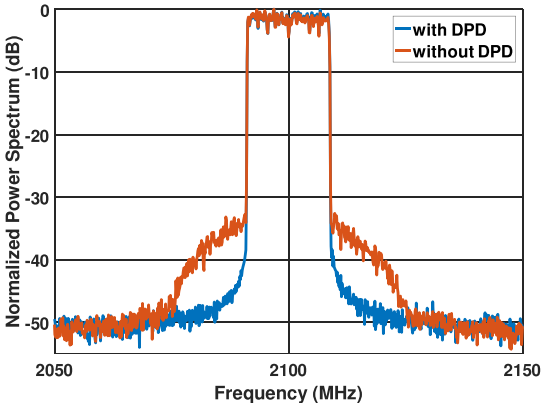
To validate the DPD performance for continuous wideband signal, the third test was carried out using a single-band signal with continuous 100-MHz instantaneous RF bandwidth. The center frequency of the test signal located at 1780 MHz.



(a)



(b)



(c)

Fig. 15. Spectra of PA outputs before and after DPD using triband LTE signals in (a) 1700, (b) 1900, and (c) 2100 MHz.

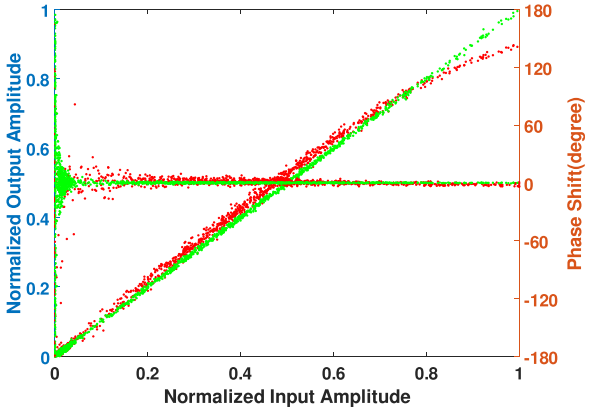


Fig. 16. AM–AM and AM–PM of PA output of triband LTE with and without proposed DPD solution.

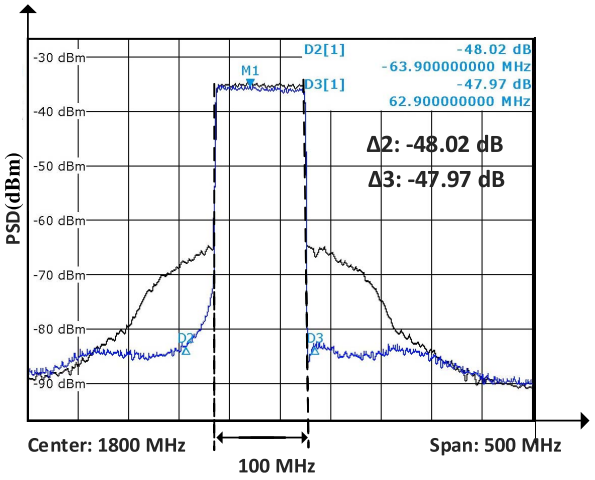


Fig. 17. Spectra of PA outputs before and after DPD using 100-MHz bandwidth signal.

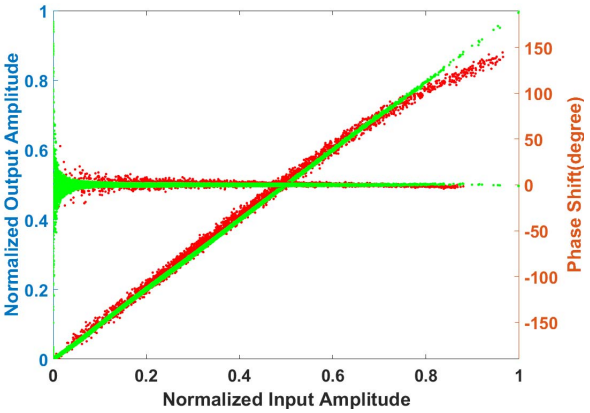


Fig. 18. AM–AM and AM–PM of PA output of 100-MHz bandwidth signal with and without proposed DPD solution.

Preliminary, the ACPR performance was achieved below −47 dB as shown in Fig. 17. The AM–AM and AM–PM performance is shown in Fig. 18. It is worth reemphasizing that we only have one low sampling rate undersampled ADC (running at 61.44 MSPS) and one BPF at the DPD sampling receiver path in those tests. At this stage, we were not trying to compete with the best wideband DPD performance in the literature. We would like to provide a feasibility validation to show that our newly proposed undersampling DPD approach (both HW and SW) can be utilized for wideband DPD application even with heavily aliased feedback signals.

E. DPD Feedback Path Usable Bandwidth Validation Test

To further validate the capability of the proposed DPD approach regarding the achievable DPD feedback path bandwidth, we reorganized the platform in the following way:

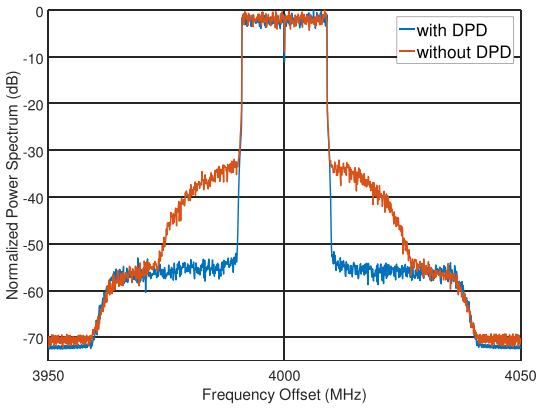


Fig. 19. Spectra of PA outputs before and after proposed DPD using a single-carrier LTE (20 MHz) at 4 GHz.

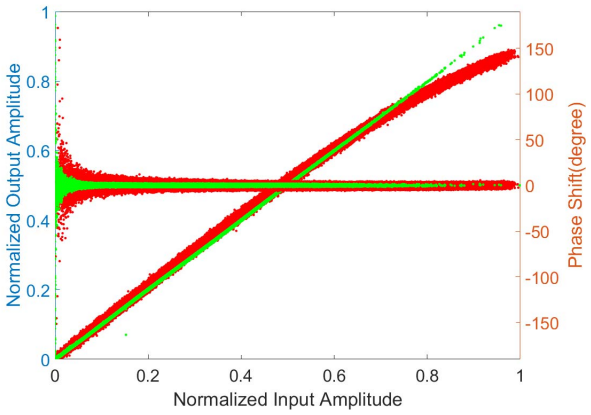


Fig. 20. AM–AM and AM–PM of PA output of 20-MHz bandwidth signal with and without proposed DPD solution at 4 GHz.

utilizing the vector signal generator R&S SMU 200 A to replace the RF-DAC at the data forward path and maintaining the single-ADC-based DPD feedback path. In this way, we can generate LTE signals at any frequency band under 6 GHz without the limitation of using certain discrete BPF, such as the RF-DAC platform. We performed a set of DPD tests at different bands. Particularly, we performed a test on a 10-W PA (CGH40010f) at 4 GHz using a 20-MHz LTE signal. Without any analog mixing stage, our proposed undersampling DPD approach achieved satisfactory −54-dBc ACPR performance using a single-ADC-based feedback path running at 61.44 MSPS, as shown in Fig. 19. In addition, we provided AM–AM and AM–PM curves, as shown in Fig. 20, for the illustration of the linearization performance as well.

VI. Conclusion

This paper presented a novel compact undersampling DPD-based PA linearization solution (including both hardware architecture and DPD algorithm) for single-chain wideband and multiband RF transmitter. Particularly, we proposed a single-ADC-based DPD sampling receiver architecture, i.e., using only one ADC with certain analog filters to replace conventional DPD feedback paths that usually include mixers or analog demodulators, LO, and middle-to-high range ADCs. By addressing several parameters of ADC and corresponding DPD algorithm, we achieved multi-GHz DPD bandwidth coverage, and demonstrated the satisfactory linearization performance of multiband and wideband RF transmitter applications via extensive experimental tests. Furthermore, the proposed undersampling ADC-based DPD feedback path can be flexibly tailored by employing different speed track-and-hold circuits for different applications, meeting various requirements of system performance and cost.

The compact architecture and algorithms presented in this paper enable a very promising efficient DPD-enabled multiband and wideband RF transmitter solution, which will play a critical role in the forthcoming green 5G wireless network.

References

[1] T. L. Marzetta, "Massive MIMO: An introduction," *Bell Labs Tech. J.*, vol. 20, pp. 11–22, Mar. 2015.

[2] L. Guan, P. Rulikowski, and R. Kearney, "Flexible practical multiband large scale antenna system architecture for 5G wireless networks," *Electron. Lett.*, vol. 52, no. 11, pp. 970–972, 2016.

[3] L. Guan and A. Zhu, "Green communications: Digital predistortion for wideband RF power amplifiers," *IEEE Microw. Mag.*, vol. 15, no. 7, pp. 84–99, Nov. 2014.

[4] J. Wood, *Behavioral Modeling and Linearization of RF Power Amplifiers*. Norwood, MA, USA: Artech House, 2014.

[5] S. A. Bassam, M. Helaoui, and F. M. Ghannouchi, "2-D digital predistortion (2-D-DPD) architecture for concurrent dual-band transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2547–2553, Oct. 2011.

[6] Y. J. Liu, W. Chen, J. Zhou, B. H. Zhou, and F. M. Ghannouchi, "Digital predistortion for concurrent dual-band transmitters using 2-D modified memory polynomials," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 281–290, Jan. 2013.

[7] L. Ding, Z. Yang, and H. Gandhi, "Concurrent dual-band digital predistortion," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3.

[8] M. Rawat, K. Rawat, M. Younes, and F. Ghannouchi, "Joint mitigation of nonlinearity and modulator imperfections in dual-band concurrent transmitter using neural networks," *Electron. Lett.*, vol. 49, no. 4, pp. 253–255, Feb. 2013.

[9] Y. Liu, J. J. Yan, H.-T. Dabag, and P. M. Asbeck, "Novel technique for wideband digital predistortion of power amplifiers with an undersampling ADC," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2604–2617, Nov. 2014.

[10] C. Yu, L. Guan, E. Zhu, and A. Zhu, "Band-limited Volterra series-based digital predistortion for wideband RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4198–4208, Dec. 2012.

[11] Y. Liu, W. Pan, S. Shao, and Y. Tang, "A new digital predistortion for wideband power amplifiers with constrained feedback bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 12, pp. 683–685, Dec. 2013.

[12] C. Yu, J. Xia, X.-W. Zhu, and A. Zhu, "Single-model single-feedback digital predistortion for concurrent multi-band wireless transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2211–2224, Jul. 2015.

[13] Z. Wang, L. Guan, and R. Farrell, "Compact undersampled digital predistortion for flexible single-chain multi-band RF transmitter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1542–1545.

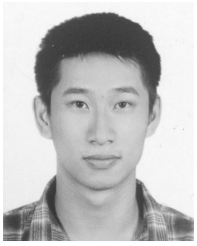
[14] Z. Wang, S. Ibrahim, H. Su, and R. Farrell, "Generalised digital predistortion of RF power amplifiers with low-rate feedback signal," in *Proc. 46th Eur. Microw. Conf. (EuMC)*, Oct. 2016, pp. 831–834.

[15] L. Guan and A. Zhu, "Optimized low-complexity implementation of least squares based model extraction for digital predistortion of RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 594–603, Mar. 2012.

[16] J. Chani-Cahuana, M. Özen, C. Fager, and T. Eriksson, "Digital predistortion parameter identification for RF power amplifiers using real-valued output data," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 10, pp. 1227–1231, Oct. 2017.

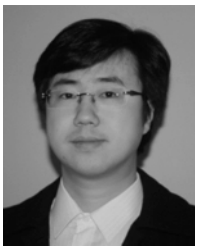
[17] P. T. Congdon, P. Mohapatra, M. Farrens, and V. Akella, "Simultaneously reducing latency and power consumption in OpenFlow switches," *IEEE/ACM Trans. Netw.*, vol. 22, no. 3, pp. 1007–1020, Jun. 2014.

[18] D. R. Morgan, Z. Ma, J. Kim, M. G. Zierdt, and J. Pastalan, "A generalized memory polynomial model for digital predistortion of RF power amplifiers," *IEEE Trans. Signal Process.*, vol. 54, no. 10, pp. 3852–3860, Oct. 2006.
[19] L. Guan and A. Zhu, "Simplified dynamic deviation reduction-based Volterra model for Doherty power amplifiers," in *Proc. Workshop Integr. Nonlinear Microw. Millim.-Wave Circuits (INMMIC)*, 2011, pp. 1–4.
[20] L. Guan, *FPGA-Based Digital Convolution for Wireless Applications*. Cham, Switzerland: Springer, 2017.
[21] *Ultra-Wideband 4 GS/s Track-and-Hold Amplifier*, Analog Devices, HMC661LC4B datasheet, v03.0615, 2017.



Ziming Wang (GS'17) received the B.Sc. degree in electrical engineering from the Wuhan University of Technology, Wuhan, China, in 2010. He is currently pursuing the Ph.D. degree in electrical engineering at Maynooth University, Maynooth, Ireland.

He joined Alcatel-Lucent, Colombes, France, for three years as a DSP Engineer. His current research interests include the design and development of low-complexity and wideband digital predistortion techniques and near antenna signal processing using the probability information of modulated signals.



Lei Guan (S'09–M'12) received the B.E. and M.E. degrees from the Harbin Institute of Technology, Harbin, China, in 2006 and 2008, respectively, and the Ph.D. degree in electronic engineering from the University College Dublin (UCD), Dublin, Ireland, in 2012.

He then spent two years involved in industrial-related research projects with UCD and Trinity College Dublin, Dublin. He is currently a Member of Technical Staff with Nokia Bell Labs, Dublin. He possesses over ten years of research and development experience in field-programmable gate arrays (FPGAs) and digital signal processing. His current research interests include RF signal conditioning algorithms for digitally assisted high-efficient RF front ends, such as digital predistortion and crest factor reduction, nonlinear system identification, software-defined radio systems, and wideband RF front ends, high-performance computing platforms, such as FPGAs and all programmable systems-on-chip, and their potentials in next-generation wireless systems, hybrid beamforming antenna array systems, large-scale antenna systems, and cloud radio access networks.

Ronan Farrell (S'99–M'93) received the Ph.D. degree in electronic engineering from the University College Dublin, Dublin, Ireland, in 1998.

Since 2000, he has been with Maynooth University, Maynooth, Ireland, where he is currently a Professor with the Department of Electronic Engineering. He is also a Co-Principal Investigator with the Science Foundation Ireland CONNECT Centre for the Internet of Things, Maynooth University. He leads a research team in the area of high-frequency radio systems with a particular interest in high-performance systems, power amplifiers, and applications of millimeter wave communications. He has co-authored over 200 journal and conference papers.