Time-Interleaved ΣΔ Modulators for FPGAs

Tomasz Podsiadlik and Ronan Farrell

***Abstract*—This brief describes and analyzes a technique of increasing a sampling rate in a sigma–delta (ΣΔ) modulator based on a discrete-time description, which is an extension of existing techniques of parallelization. The limitations in the signal-to-noise ratio and the maximum increase of the sampling rate in a digital system are explained, and a structure of a low-pass ΣΔ modulator characterized by a short critical path is used in this brief to validate the technique. An implementation of a modulator shows the increase in the sampling rate from 100 to 400 MHz.**

***Index Terms*—Sampling frequency, sigma–delta (ΣΔ), time interleaved (TI).**

I. Introduction

SIGMA–DELTA ($\Sigma\Delta$) modulators are known for their capability for encoding an analog or a multibit digital input signal into a two- or multilevel signal while preserving a high signal-to-noise ratio (SNR). While the use of a two-level quantizer improves linearity of a digital-to-analog converter, it also adds a significant level of quantization noise. Apart from the order and number of levels, the most important factor limiting the SNR in the output of a $\Sigma\Delta$ modulator is the oversampling ratio (OSR). While the demand for $\Sigma\Delta$ operation above 1-GHz clock rates can be found in wireless communication [1], such high speed cannot be delivered by modern field-programmable gate arrays (FPGAs) without utilizing their resources in parallel. A simple method of utilizing $\Sigma\Delta$ modulators in parallel is shown in Fig. 1(a). The modulator operating at a low sampling rate f_S is replicated N times, and each of the parallel blocks is fed with consecutive input samples. The outputs of the parallel blocks are next upsampled and added, creating the sequence sampled at increased rate Nf_S, with large N possible. The drawback of the direct technique is that the noise transfer function (NTF) of the modulator is the same as the NTF of the modulator operating at a low sampling rate, repeated in the frequency domain every f_S, as depicted in Fig. 1(b) [2]. Consequently, the parallel modulator shows only 3 dB of SNR improvement per every doubling of N, whereas at least 9 dB of improvement is expected, i.e., 9 dB for a first-order modulator or more when a higher order modulator is used. In order to preserve the desired NTF of Fig. 1(c), more advanced techniques of parallelization are needed. A time-interleaved (TI) $\Sigma\Delta$ modulator using a block digital filter technique was proposed by Khoini-Poorfard *et al.* [3]. They used a multirate system for replacing loop filters in a $\Sigma\Delta$ modulator, which reduced the sampling rate of the digital hardware N times while preserving the same NTF and signal transfer function (STF) of the original modulator. The drawback of the block digital filter TI$\Sigma\Delta$ is a large hardware count caused by $N-1$ cross connections between each of the parallel branches. The problem of large hardware count was alleviated by Kozak and Kale, who derived a TI$\Sigma\Delta$ modulator by using node equations of a conventional $\Sigma\Delta$ modulator [4]. The technique uses a system of discrete-time-domain equations to describe a $\Sigma\Delta$ modulator, which are next written for N consecutive time slots. After combining them into a one system, one arrives at a time-domain description of the TI$\Sigma\Delta$ modulator. To the authors' knowledge, despite the advantages of the technique, its implementation in digital hardware has not been presented to date.

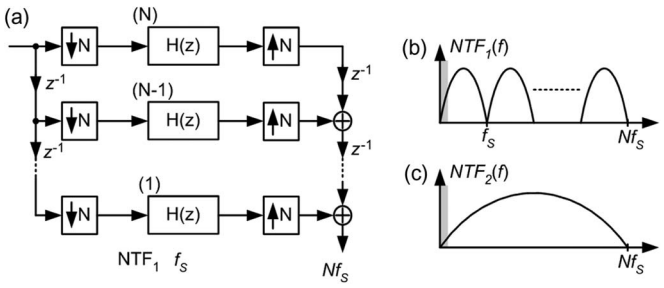

Fig. 1. Parallel modulator. (a) N blocks in parallel. (b) NTF of the parallel modulator. (c) Desired NTF.

This brief describes a method for designing a TI$\Sigma\Delta$ modulator based on discrete-time-domain equations, close in a concept to this presented in [4]. Section II discusses structures of $\Sigma\Delta$ modulators suitable for operation at a high sampling rate. Section III describes the proposed technique, and a TI modulator based on a cascaded integrator with distributed feedback (CIFB) structure is presented and studied in Sections IV and V. Experimental results are presented in Section VI. Section VII concludes this brief.

II. CP in ΣΔ Modulators

This section addresses the problem of critical path (CP) in low-pass (LP) and bandpass $\Sigma\Delta$ modulators structures using a CIFB and a cascade of resonators with distributed feedback (CRFB) [5]. Every gate in a combinational circuit induces a propagation delay between its input and output caused by the response time of transistors to changing voltage levels. The path with the longest propagation time, i.e., the CP, limits the maximum clock frequency that the filter can operate at. Often an LP$\Sigma\Delta$ modulator whose NTF zeros are superimposed at $z=1$, such as the CIFB structure shown in Fig. 2(a), can be composed of first-order sections, e.g., integrators $H_{1,2,\ldots}(z)=z^{-1}/(1-z^{-1})$ in the CIFB modulator, which yield the numerator of the

Manuscript received January 25, 2014; revised May 25, 2014; accepted July 30, 2014. Date of publication August 1, 2014; date of current version October 1, 2014. This work was supported by Science Foundation Ireland under Grant 03/CE3/I405. This brief was recommended by Associate Editor L. H. Corporales.

T. Podsiadlik is with Benetel Ltd., Dublin, Ireland (e-mail: tomaszpodsiadlik@benetel.com).

R. Farrell is with National University of Ireland, Maynooth, Ireland (e-mail: rfarrell@eeng.nuim.ie).

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Digital Object Identifier 10.1109/TCSII.2014.2345293

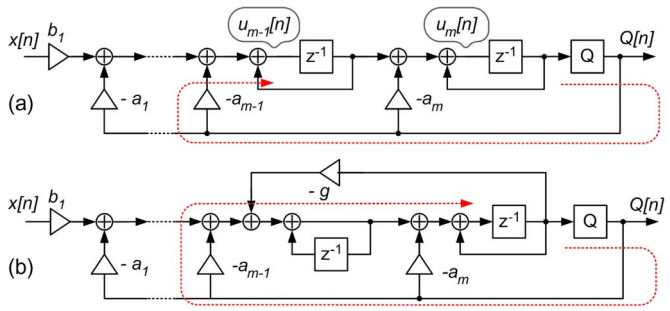

Fig. 2. (a) Arbitrary-order CIFB ΣΔ. (b) Arbitrary-order CRFB ΣΔ.

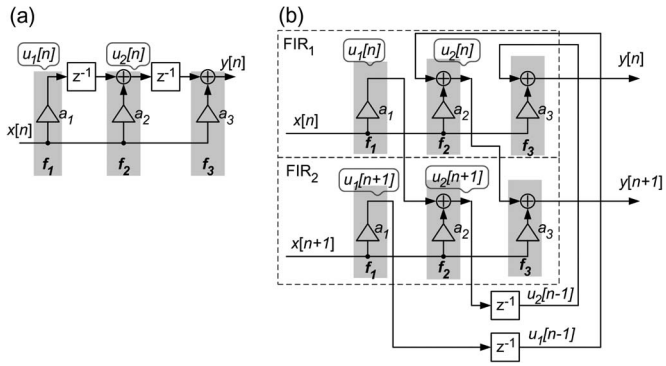

Fig. 3. (a) Second-order FIR filter. (b) Parallel expansion.

NTF in the form of $\mathrm{NTF}_{\mathrm{NUM}} = (1 - z^{-1})(1 - z^{-1}) \ldots$. It is observed that the CP marked by the dashed line in Fig. 2(a) consists of one quantizer, one multiplier, and two adders only. In addition, an expansion to a higher order by adding more of the delaying integrators has no effect on the length of the CP. Consequently, the LPΣΔ modulators are usually suitable for operation at high clock frequencies. The advantage of the low complexity in the CP is, however, bought at the cost of restraining the modulator to LP or high-pass operation only, i.e., NTF zeros can be either $z = 1$ or $z = -1$. On the other hand, a band-pass operation requires that the zeros in the NTF are located at some positive frequency $0 < f < f_{\Sigma\Delta}/2$. Such zeros can be obtained when the numerator of NTF is in the form of a product of quadratic equations: $\mathrm{NTF}_{\mathrm{NUM}} = \left(1 - a_1 z_1^{-1} + z^{-2}\right)(1 - a_2 z^{-1} + z^{-2}) \ldots$. The necessity of the use of at least second-order sections instead of first-order sections such as in the LPΣΔ modulator causes the increase of a CP, which is observed in the CRFB structure. The CP in the modulator consists of five adders, a multiplier, and a quantizer in cascade.

III. TIΣΔ Modulators in the Time Domain

This section describes a method of a parallel expansion based on discrete-time-domain equations of a ΣΔ modulator. The technique described in this section aims in increasing a sampling frequency of an LPΣΔ modulator, although it is not limited to LP operation only.

A ΣΔ modulator or a digital filter can be described at a current time index n by its state variables being a function(s) of a current and delayed variables at discrete times: $n, n-1, n-2 \ldots$. When the circuit is time invariant, then the variables at subsequent time steps can be found by increasing n in the equations. For instance, a second-order finite-impulse response (FIR) filter shown in Fig. 3(a) can be described at time index n by

$$\begin{aligned} u_1[n] &= a_1 x[n] \\ u_2[n] &= a_2 x[n] + u_1[n-1] \\ y[n] &= a_3 x[n] + u_2[n-1]. \end{aligned} \tag{1}$$

The next state is found by transforming $n \to n+1$ in (1), i.e.,

$$\begin{aligned} u_1[n+1] &= a_1 x[n+1] \\ u_2[n+1] &= a_2 x[n+1] + u_1[n] \\ y[n+1] &= a_3 x[n+1] + u_2[n]. \end{aligned} \tag{2}$$

The two systems of equations (1) and (2) are used to derive the block diagram of two FIR filters in parallel, computing consecutive filter outputs at times n and $n+1$, as shown in Fig. 3(b). The first section marked as FIR_1 computes variables u_1, u_2, and y at discrete time n, i.e., it implements system of equations (1). Subsequently, $u_1[n]$ and $u_2[n]$ computed by FIR_1 are fed to FIR_2 and used to compute variables at discrete time $n+1$, implementing (2). If the propagation delays in the expanded system are sufficiently short to compute u_1, u_2, and y at both time indexes n and $n+1$ before the end of clock period $T_S = 1/f_S$, then the sampling rate of the expanded system can be increased 2 times in comparison with the basic structure of the filter shown in Fig. 3(a). In a general case, a discrete-time ΣΔ modulator can be described at time n by a system of discrete-time equations, being functions of variables at discrete times $n, n-1, n-2, \ldots$, etc.,

$$\begin{aligned} y[n] &= f_1\left(x[n]\, u_1[n-1],\, u_2[n-1] \ldots\right) \\ u_1[n] &= f_2\left(x[n]\, u_1[n-1],\, u_2[n-1] \ldots\right) \\ u_2[n] &= f_3\left(x[n]\, u_1[n-1],\, u_2[n-1] \ldots\right) \\ &\ldots \end{aligned} \tag{3}$$

The expansion into the TI circuit is obtained in three steps. First, the system of discrete-time equations is written for N consecutive time indexes: $N \cdot n, N \cdot n + 1, N \cdot n + 2, \ldots, N \cdot n + N - 1$. In the second step, the N systems of equations are used to create N digital subsystems. In the third step, the subsystems are cross connected according to the discrete-time-domain equations. The resulting TI circuit supplied with N consecutive inputs returns N consecutive outputs during a single clock cycle, increasing the effective sampling rate of the modulator N times. After the Nth computation, the variables are fed back in the circuit through delay blocks.

In theory, the discrete-time ΣΔ modulator can be expanded to any number N of blocks in parallel using the method described earlier in this brief. In practice, every increase of the number of sections in parallel causes increase of the computation time in the CP. The maximum number of blocks in parallel N is thus limited, and it can be found as $N_{\mathrm{MAX}} \approx T_S/T_C$, where T_S is the clock period of the TI system and T_C is the computation time in the CP of the original structure.

IV. Sample-and-Hold TIΣΔ Modulator

This section describes a TI expansion of an arbitrary-order CIFB LPΣΔ modulator, in which a large OSR typical for

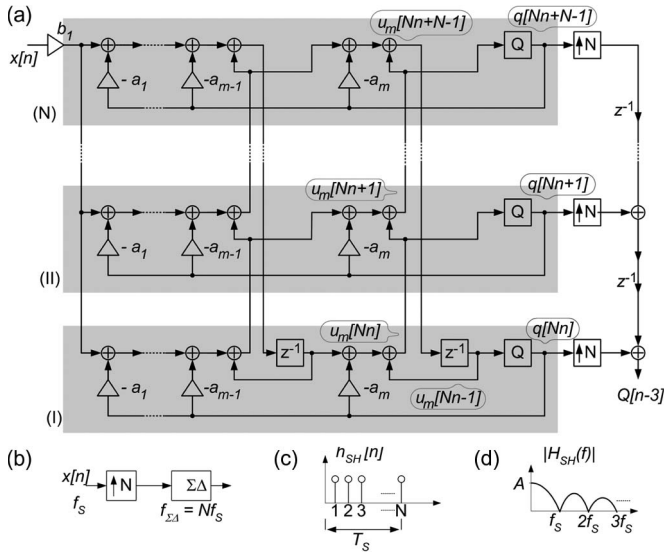

Fig. 4. (a) Sample-and-hold TIΣΔ using the CIFB structure. (b) Equivalent system. (c) Impulse response of the expander. (d) Magnitude response of the expander.

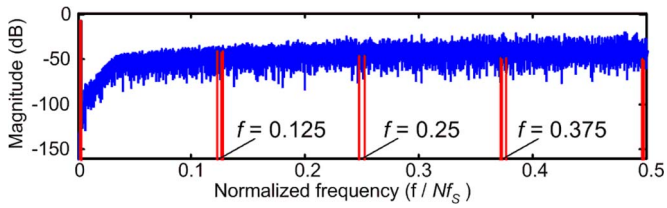

Fig. 5. Simulated spectrum of a third-order sample-and-hold TIΣΔ modulator.

two-level modulators is exploited for reducing complexity of the TIΣΔ structure.

The CIFB ΣΔ modulator of order m is shown in Fig. 2(a) and it is described in the time domain by

$$\begin{aligned} q[n] &= Sgn\{u_m[n-1]\} \\ u_1[n] &= b_1 x[n] - a_1 q[n] + u_1[n-1] \\ u_m[n] &= u_{m-1}[n-1] - a_m q[n] + u_m[n-1]. \end{aligned} \tag{4}$$

Using $n \to Nn$ transformation in the first block in parallel, and $n \to Nn+1$ transformation in every subsequent subsection, the time-domain equations at consecutive n are obtained. The equations for the first (I) and second (II) parallel sections, respectively, are given as

$$\begin{aligned} q[Nn] &= Sgn\{u_m[Nn-1]\} \\ u_1[Nn] &= b_1 x[Nn] - a_1 q[Nn] + u_1[Nn-1] \\ u_m[Nn] &= u_{m-1}[Nn-1] - a_m q[Nn] + u_m[Nn-1] \end{aligned} \tag{5}$$

$$\begin{aligned} q[Nn+1] &= Sgn\{u_m[Nn]\} \\ u_1[Nn+1] &= b_1 x[Nn+1] - a_1 q[Nn+1] + u_1[Nn] \\ u_m[Nn+1] &= u_{m-1}[Nn] - a_m q[Nn+1] + u_m[Nn]. \end{aligned} \tag{6}$$

TABLE I
NTF ZEROS AND POLES. ALL MODULATORS USED $\|\text{NTF}_\infty\| = 1.5$

Ord	Zeros	Poles
2	$z_{1,2} = 1$	$p_{1,2} = 0.61 \pm j0.26$
3	$z_{1,2,3} = 1$	$p_{1,2} = 0.77 \pm j0.28$ $p_3 = 0.67$
4	$z_{1,2,3,4} = 1$	$p_{1,2} = 0.85 \pm j0.25$ $p_{3,4} = 0.75 \pm j0.088$

Taking advantage of the high OSR, the demultiplexer composed of delays and decimators for distributing the input samples in TI modulators, e.g., as shown in Fig. 1(a), can be reduced to a single input sampled at the low rate $f_S = f_{\Sigma\Delta}/N$ and supplied to all parallel blocks. The hardware-reduced modulator is shown in Fig. 4. The above simplification is equivalent to the upsampling of the input signal by a factor of N with repetition of the input samples, as shown in Fig. 4(b) and (c). In consequence of the reduced input sampling rate, aliases of the input signal occur at frequencies $m(f_{\Sigma\Delta}/N),\ m = \pm 1, \pm 2, \ldots$. As these frequencies coincide with zero frequencies of the discrete-time Fourier transform from h_{SH} shown in Fig. 4(d), the aliases are suppressed by the H_{SH} function and have their magnitudes usually below the quantization noise. Their effect on the SNR in a TI modulator is therefore small. This can be seen in the simulated spectrum for the third-order LPΣΔ modulator shown in Fig. 5 for $N = 8$.

Third- and fourth-order TIΣΔ modulators whose NTF zeros/poles are given in Table I were simulated with a two-tone input and OSR $= 200$. Both third- and fourth-order TIΣΔ showed maximum SNRs of 111.4 and 131.4 dB, respectively, when $N = 16$, yielding nearly the same SNR as ideal modulators.

V. ZERO INSERTION IN THE TIΣΔ MODULATOR

Further simplification to the TIΣΔ can be achieved when the zero-insertion technique proposed in [4] is used. The TIΣΔ modulator with zero insertion is created by providing an input at low sampling rate $f_S = f_{\Sigma\Delta}/N$ to one parallel section only and by setting zero inputs for remaining ones, as shown in Fig. 6(a), for the CIFB modulator. This technique allows for reducing the hardware count of the TIΣΔ modulator by at least one multibit adder in each parallel section apart from the first one. Not entirely correct, in [4], the occurrence of aliases was explained as having a negligible impact on the SNR of a zero-insertion TIΣΔ (ZI-TIΣΔ) modulator since magnitudes of the aliases should be well below a ΣΔ quantization noise. The above explanation is, however, rarely true. The effect of the zero insertion on the SNR performance and the use of LP-STF for preventing the degradation are explained in this section.

A. Effect of High N on the SNR in ZI-TILPΣΔ

The ZI-TIΣΔ can be modeled as a modulator operating at the high sampling rate $f_{\Sigma\Delta} = Nf_S$, whose input signal sampled at the low rate $f_S = f_{\Sigma\Delta}/N$ is supplied to the modulator through an expander, as shown in Fig. 6(b). The expander has impulse and magnitude responses depicted in Fig. 6(c) and (d), respectively. The output of the expander consists of a baseband portion of the input signal and aliases at frequencies $m(f_{\Sigma\Delta}/N)$, similar to the sample-and-hold technique. The difference is that

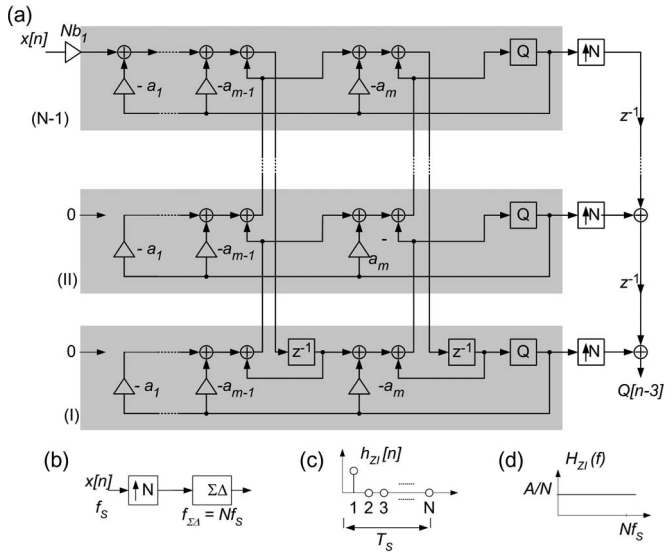

Fig. 6. (a) ZI-TIΣΔ modulator based on the CIFB structure. (b) Equivalent scheme. (c) Impulse response of the expander. (d) Magnitude response of the expander.

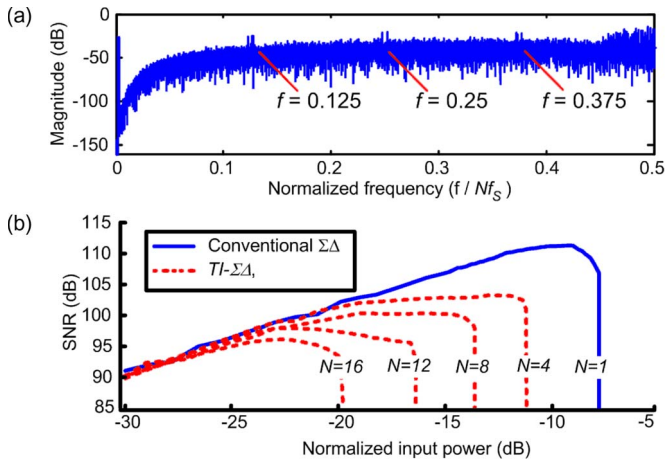

Fig. 7. Simulated third-order TI-LPΣΔ—flat STF. (a) Output spectrum for $N = 8$. (b) SNR as a function of N.

now all of the components have the same magnitudes due to the flat response of the expander, and they are equal to $1/N$ of the input magnitude before the expander. Consequently, the input gain to the modulator should be increased N times, as shown in Fig. 6(a). Because the total input power to the modulator increases N times, subsequent reduction of the modulators' stable input range and maximum SNR is expected. The presence of aliases at frequencies $f = (1/8)f_{\Sigma\Delta}$, $f = (2/8)f_{\Sigma\Delta}$, $f = (3/8)f_{\Sigma\Delta}$, and $f = (4/8)f_{\Sigma\Delta}$ are observed in the simulated spectrum of the third-order modulator for $N = 8$ in Fig. 7(a), whose STF $= 1$ and NTF has zeros/poles listed in Table I The progressive reduction of the SNR caused by increasing N is clearly seen in Fig. 7(b), showing the simulation performed for the third-order modulator. This effect is common for other ZI-TIΣΔ.

B. ZI-TIΣΔ Modulator With LP-STF

To take full-advantage of the reduced hardware complexity in the ZI-TIΣΔ modulator, the aliases of the input signal

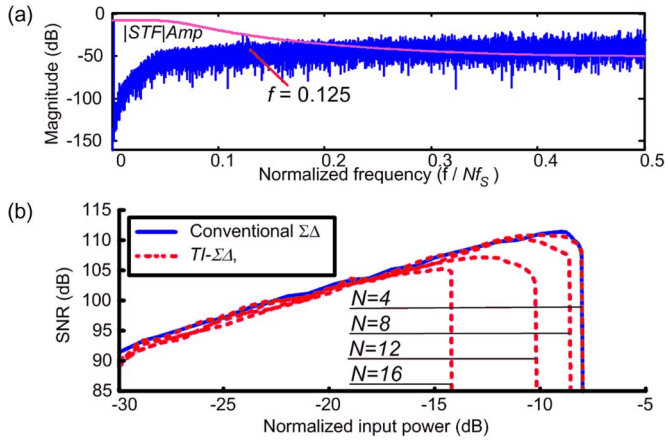

Fig. 8. Simulated third-order TI-LPΣΔ—LP-STF. (a) Output spectrum for $N = 8$. (b) SNR as a function of N.

TABLE II
SNR DEGRADATION (ΔSNR) IN ZI-TIΣΔ FOR FLAT LP-STF

ΣΔ	$SNR\,(dB)$	$\Delta SNR\,(dB)$		
Ord	$N = 1$	$N = 4$ $Flat/LP$	$N = 8$ $Flat/LP$	$N = 16$ $Flat/LP$
2	86.4	7/0.2	11/4	14.3/8.2
3	111.4	8.5/1	11/1.2	14.4/5.4
4	131.4	8.44/0.4	10.9/1	15.4/3.8

should be suppressed in the course of the ΣΔ modulation. As a common practice, the NTF poles for the LPΣΔ modulator are often obtained as the poles of a Butterworth filter [5]. In result, modulators whose STF and NTF share the same poles, such as CIFB or CRFB, have LP-STF with a similar frequency response to that of the Butterworth filter, enabling suppression of the aliases in the output of the expander. Unfortunately, the cutoff frequency of the STF cannot be chosen freely, and it is determined by NTF, imposing some limitation toward the suppression of the input aliases. In general, the cutoff frequency decreases as the order of ΣΔ increases. Fig. 8(a) shows a simulated output spectrum and the effect of LP-STF. The SNR calculated for a third-order ZI-TIΣΔ modulator is presented in Fig. 8(b) for a two-tone input and OSR $= 200$. The modulator with LP-STF has its stable range and SNR close to the modulator operating at 4 times higher sampling rate and a higher maximum SNR for all N than a modulator with STF $= 1$, which is observed when comparing Figs. 7(b) and 8(b). The summary of the maximum SNR in the simulated modulators and the SNR degradation in ZI-TIΣΔ is provided in Table II for second-, third-, and fourth-order ΣΔ modulators. All modulators had NTF with $\|H_{\mathrm{INF}}\| = 1.5$. Both TI modulators, using STF $= 1$ and LP-STF, are simulated with OSR $= 200$ and a two-tone input. The suppression of the aliases gradually improves when increasing the order of the Butterworth filter, which is observed for $N = 8$, $N = 16$, and it is an expected result.

VI. EXPERIMENTAL RESULTS AND DISCUSSION

This section validates the technique of expansion to a TIΣΔ modulator, providing simulated and measured results for modulators implemented in Virtex 2 Pro FPGA of Xilinx.

The increase of sampling rate in LPΣΔ modulators implemented in FPGAs can be achieved either by multiplication of

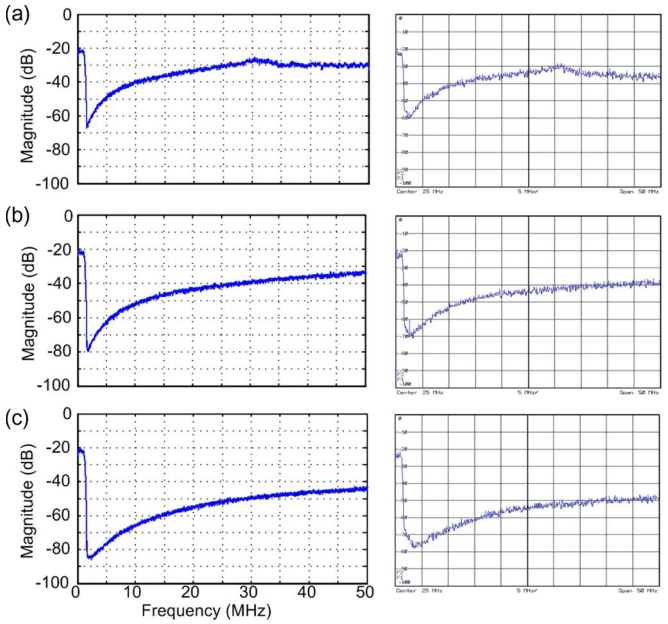

Fig. 9. Second-order $\Sigma\Delta$ modulator: (left) simulated and (right) measured. (a) $f_S = 100$ MHz. (b) $N = 2$, $f_S = 200$ MHz. (c) $N = 4$, $f_S = 400$ MHz.

a clock frequency while using a conventional $\Sigma\Delta$ modulator or by employing the TI technique described in this brief. Two observations are made when comparing both approaches. 1) Provided the same effective sampling rate in both approaches, the TI modulator uses more hardware for computing consecutive outputs, but the total number of arithmetic operations performed during N clock cycles remains the same. Moreover, both approaches use the same number of delay elements, but they are written N times less frequently in the TI$\Sigma\Delta$, implying less power consumption in the latter. 2) The analysis of the time-domain equations at consecutive times shows that the CP reduction in a TI$\Sigma\Delta$ modulator is possible at the cost of a minor hardware increase. Consequently, the CP computation becomes less than NT_C in the TI$\Sigma\Delta$. For instance, the CP can be reduced by one addition per every consecutive output in a first-order sample-and-hold TI$\Sigma\Delta$ in comparison with the same-order conventional modulator. Similar CP reductions are possible in higher order modulators. The implemented TI$\Sigma\Delta$ modulators of orders 1 and 2 with $N = 4$ allowed over 30% higher sampling rate than equivalent conventional modulators.

The implemented modulators were supplied with a baseband signal having a bandwidth BW $= 1.25$ MHz. The input sequence was sampled at the rate of $f_S = 50$ MHz, and a simple sample-and-hold method was used for increasing the sampling rate to the rate of $\Sigma\Delta$ modulators. The FPGA used a 100-MHz clock signal. The output multiplexer was implemented with the use of a *Rocket IO* transceiver operating as a 20-bit parallel-to-serial register. The serial output from the FPGA board was connected to a spectrum analyzer FSL of *Rohde & Schwarz*. The implemented structures were second-order CIFB, LP$\Sigma\Delta$ modulators for $N = 1$ (100 MHz), $N = 2$ (200 MHz), and $N = 4$ (400 MHz). The simulated outputs of second-order TI$\Sigma\Delta$ modulators show a dynamic range of improvement of approximately 14 dB per doubling of the sampling rate, as shown in Fig. 9(a) and (b), which is in a close agreement with the expectation [5], whereas some degradation in the dynamic range caused by 11 bit wordlength used in the simulation is shown to observed Fig. 9(c) for $N = 4$. The graphs on the right-hand side show the measured spectra from the output of the Virtex II Pro FPGA board. The measured results resemble the simulated modulators outputs for $f_{\Sigma\Delta} = 100$ MHz and $f_{\Sigma\Delta} = 200$ MHz. Some degradation in dynamic range to the simulated spectrum is observed at low frequencies when $f_{\Sigma\Delta} = 400$ MHz. The distortion has been caused by a jitter added by the phase-locked loop in *Rocket IO* of the FPGA and by the memory effect in the output 1-bit digital-to-analog converter. The implemented modulators prove the concept of the parallel expansion technique presented in this brief and show an increase of the sampling rate in comparison with conventional modulators implemented in the same, or newer generations of FPGAs: $f_{\Sigma\Delta} = 100$ MHz for the error feedback topology [6] in Virtex II Pro, $f_{\Sigma\Delta} = 215$ MHz for the second-order CRFB structure implemented in Virtex II Pro [9], and $f_{\Sigma\Delta} = 219$ MHz for the second-order CRFF structure implemented in Virtex 6 [8].

VII. Conclusion

This brief has demonstrated a technique of parallelizing $\Sigma\Delta$ modulators, being an extension to existing techniques [4]. Mechanisms affecting maximum sampling frequency and SNR in TI$\Sigma\Delta$ modulators were explained, and the concept was validated through experimental results employing *Virtex II Pro* FPGA, showing the increase of a sampling rate by factor of four. The TI$\Sigma\Delta$ can be employed in wireless communication where two $z \to -z$ transformed TI$\Sigma\Delta$ modulators operate at increased $2f_{\Sigma\Delta}$ frequency creating a bandpass drive signal for switch-mode power amplifiers [10].

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